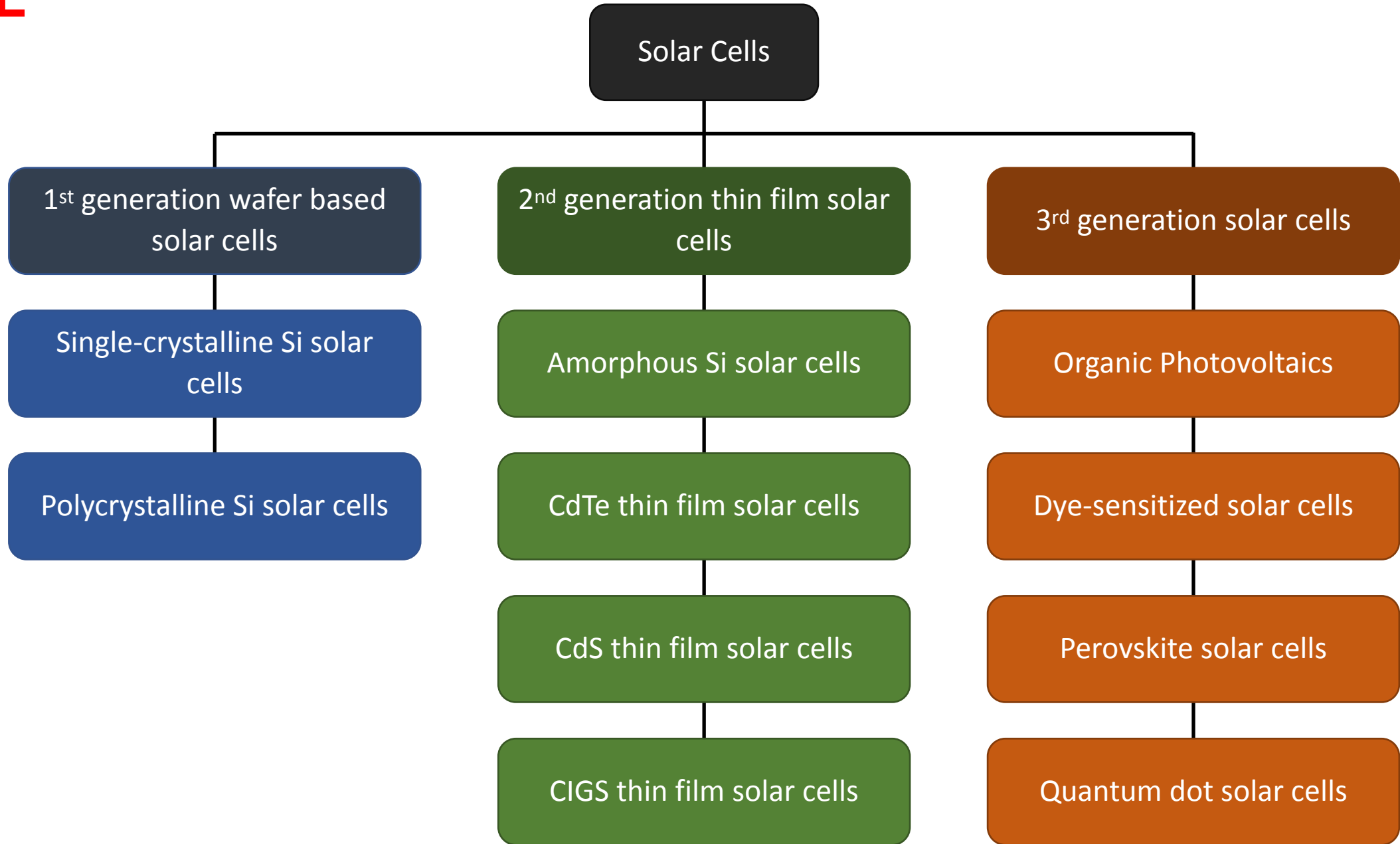


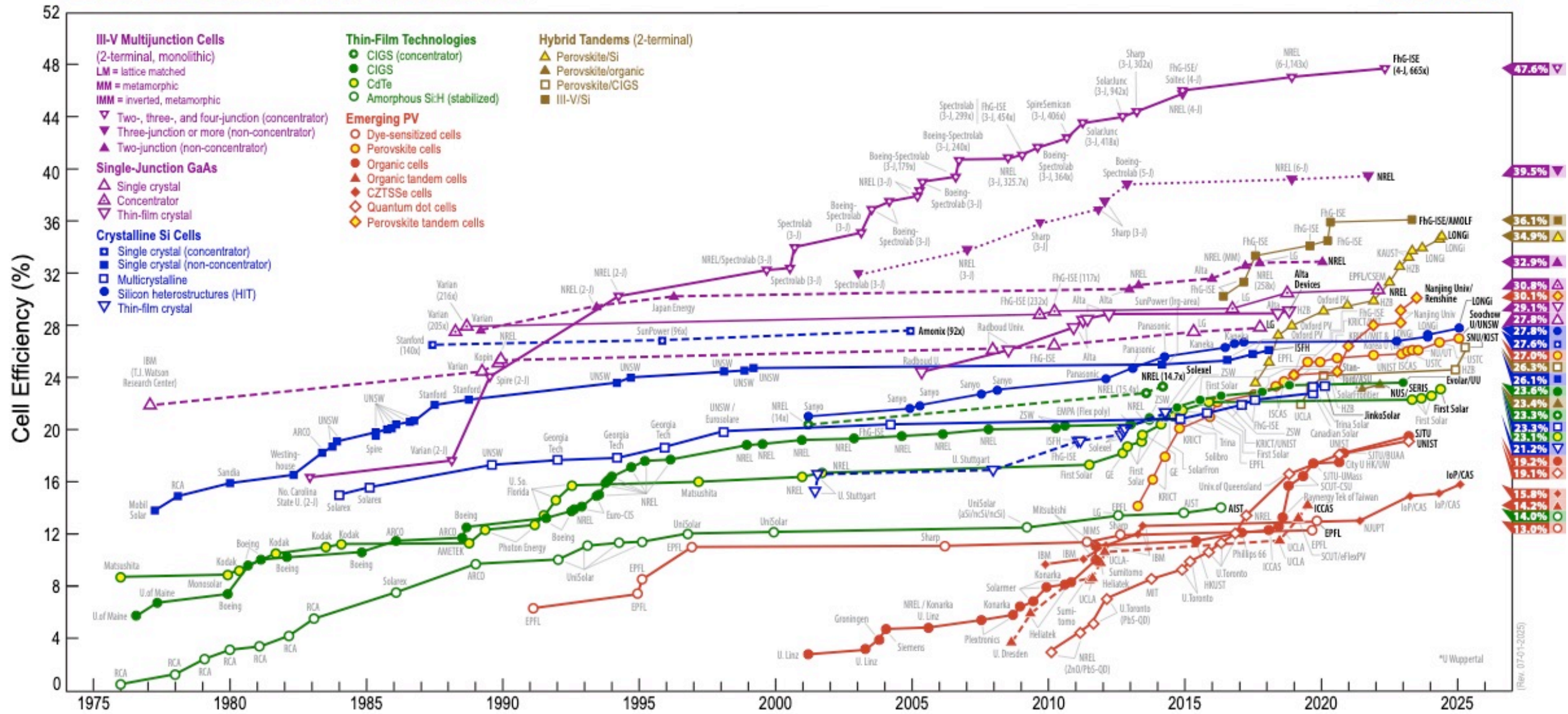
Energy Conversion by Semiconductor Devices

Jun-Ho YUM

junho.yum@epfl.ch

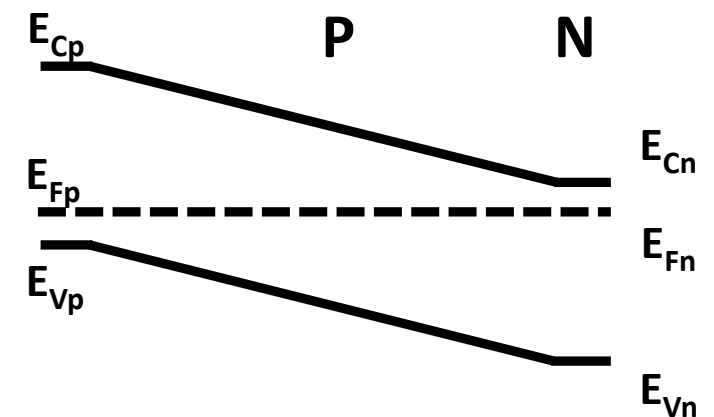
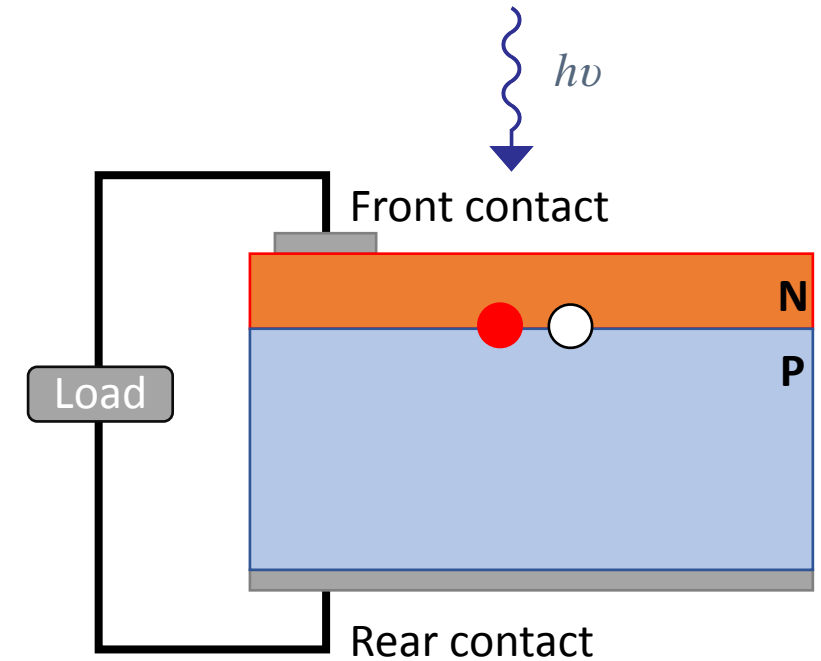


Best Research-Cell Efficiencies



EPFL pn Junction Solar Cell

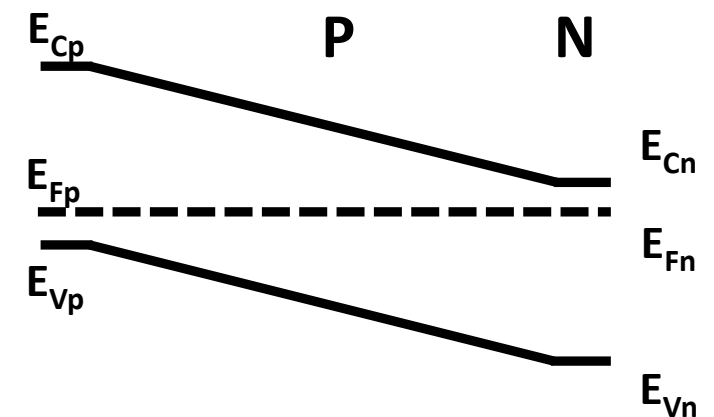
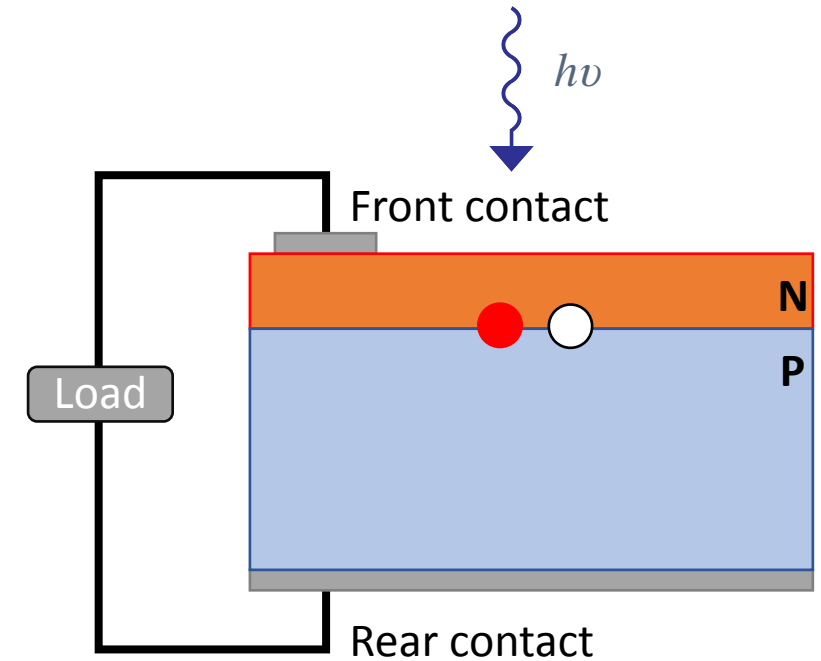
- In general, the n region is heavily doped and thin so that the light can penetrate through it easily.
- The p region is lightly doped so that most of the depletion region lies in the p side.
- Main two processes: carrier generation and carrier collection.
- Electron-hole pairs are generated by the incident photon $> E_g$.
- The carriers are separated by the E-field existing at the p-n junction.
- The electron-hole pairs exist, on average, for a length of time equal to the minority carrier lifetime before they recombine.



See the animation in <https://www.pveducation.org/pvcdrom/solar-cell-operation/light-generated-current>

EPFL pn Junction Solar Cell

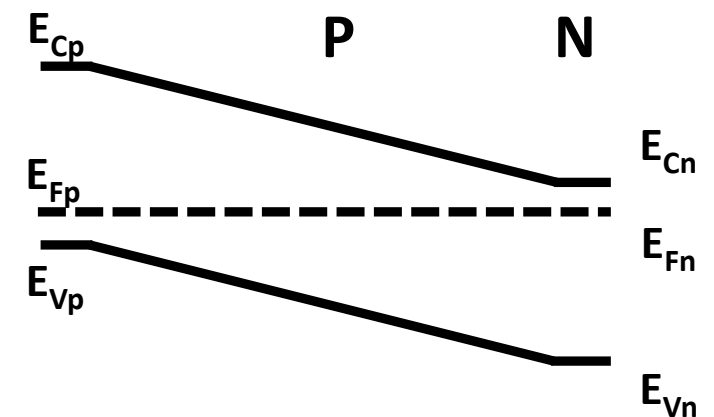
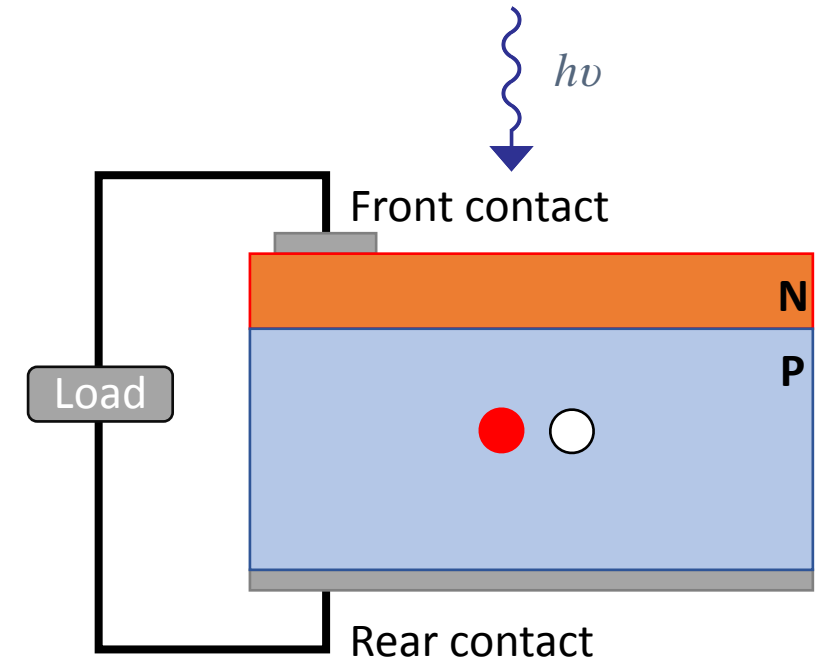
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EPFL pn Junction Solar Cell

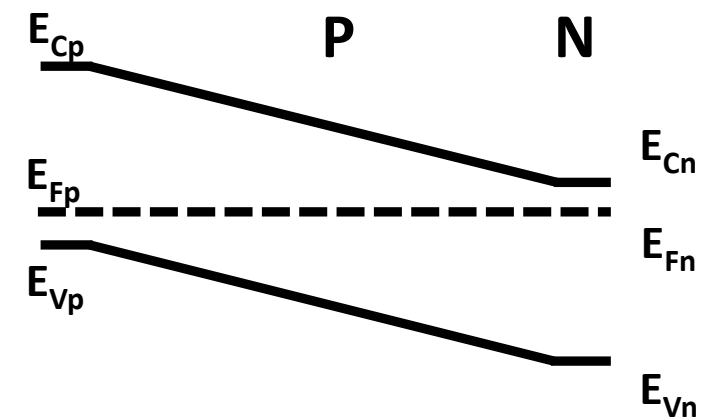
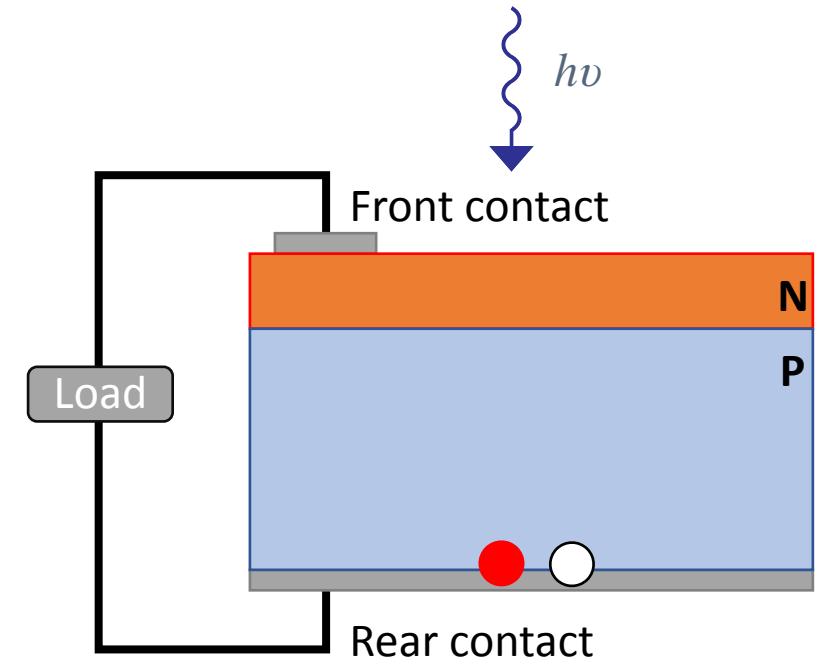
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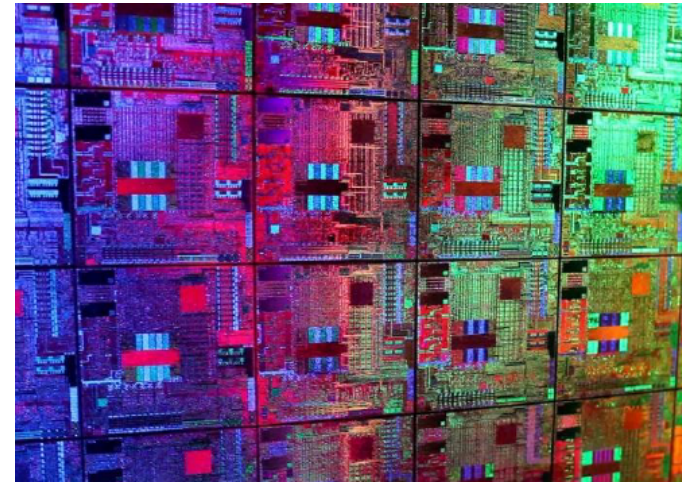
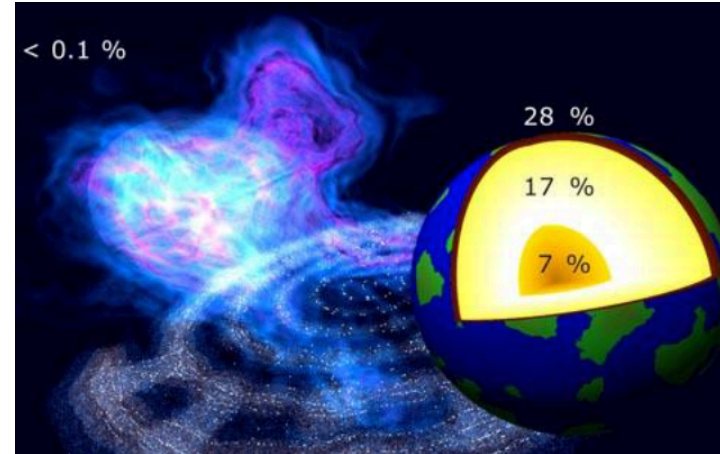
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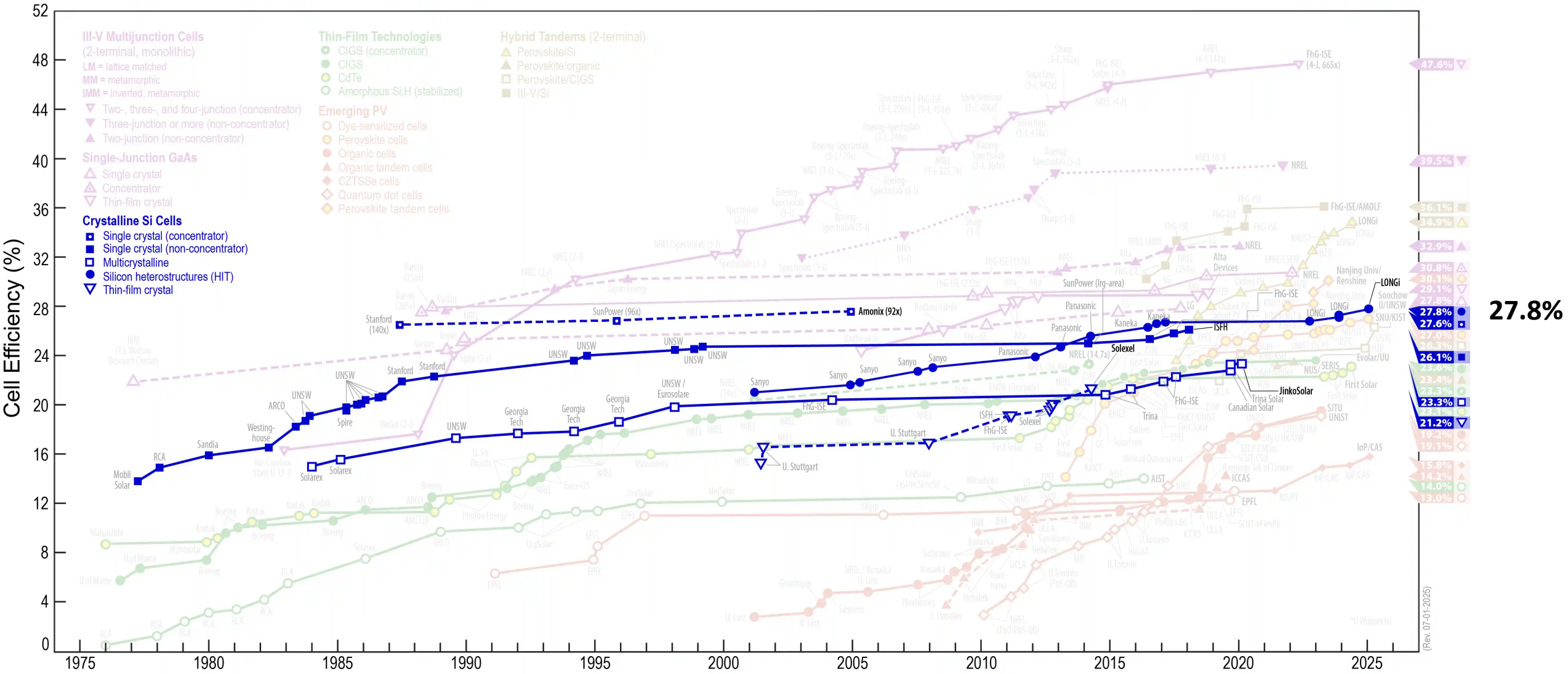


See the animation in <https://www.pveducation.org/pvcdrom/solar-cell-operation/light-generated-current>

Si has suitable E_g , 1.12 eV
Doing is possible
Abundant and non-toxic
Mostly used in microelectronics

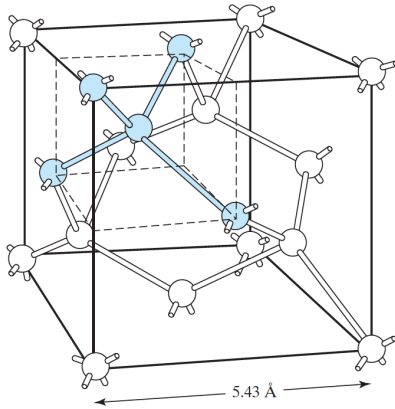


Best Research-Cell Efficiencies

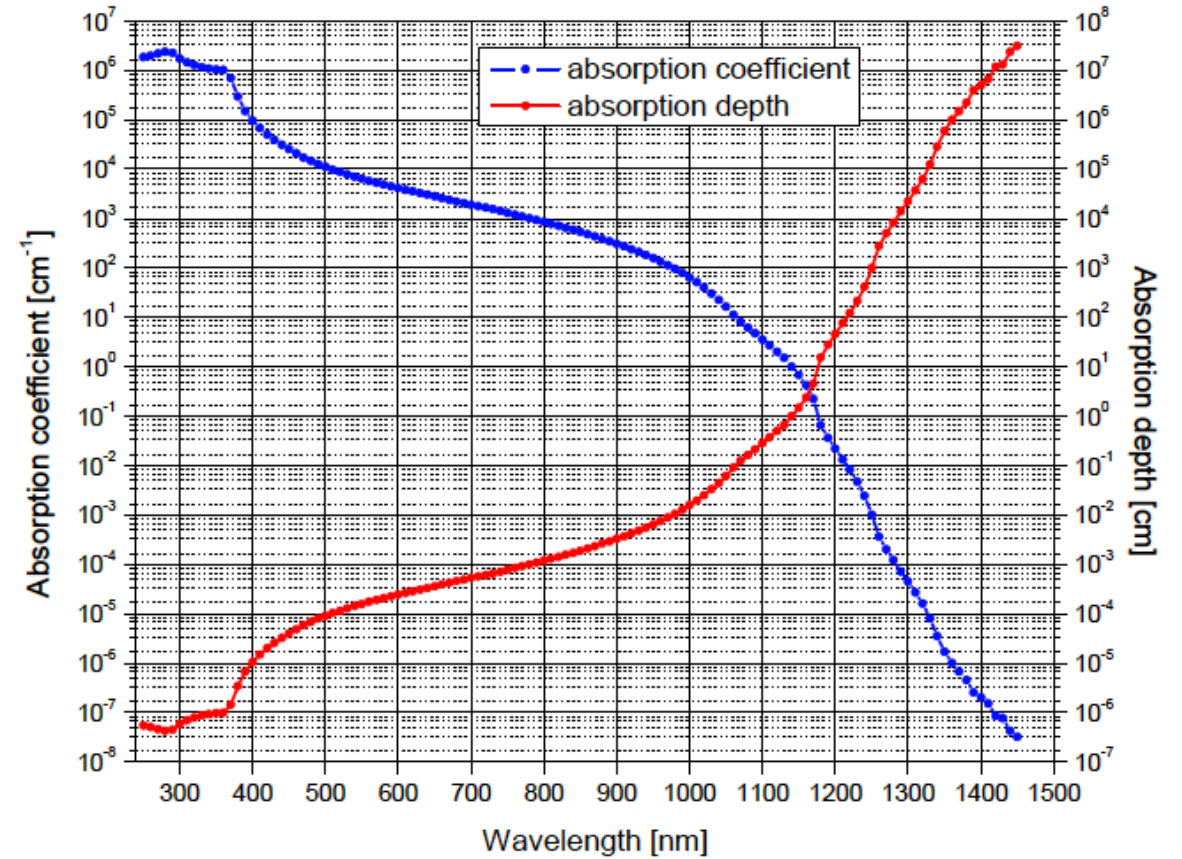
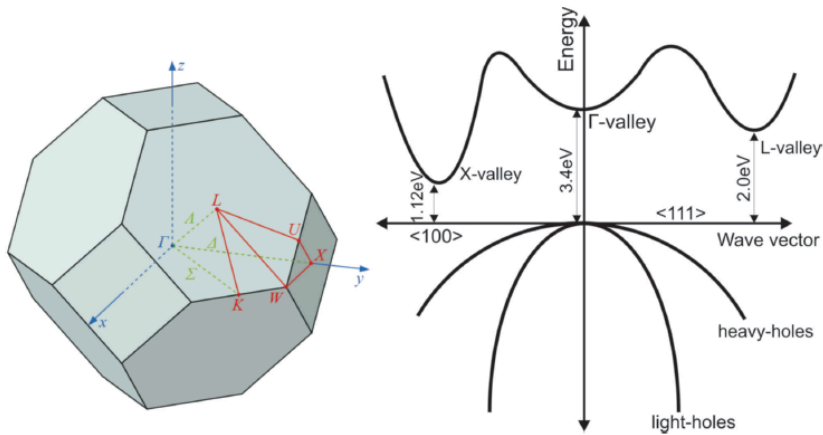


EPFL Crystalline Silicon

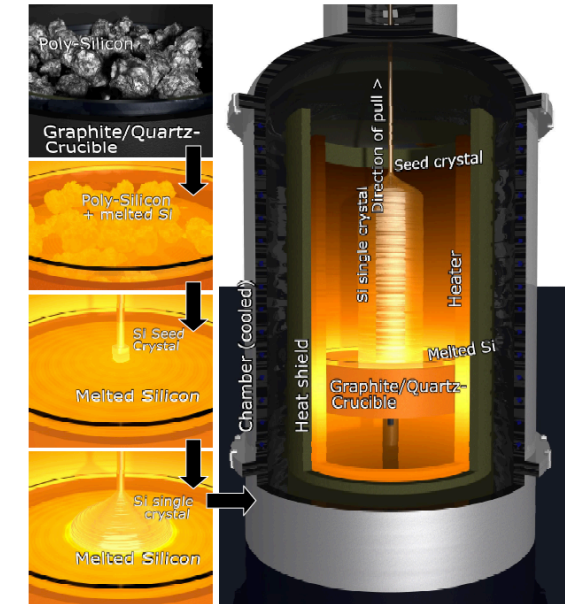
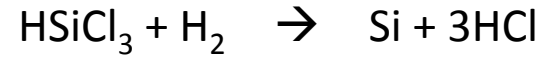
Bond angle is $109^{\circ}28'$ and bond length is approximately 2.35 \AA .



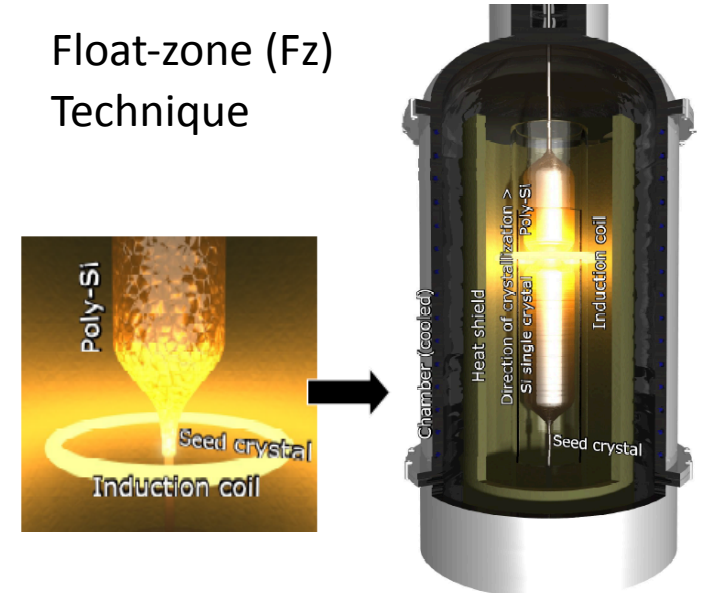
Indirect band gap is 1.12 eV



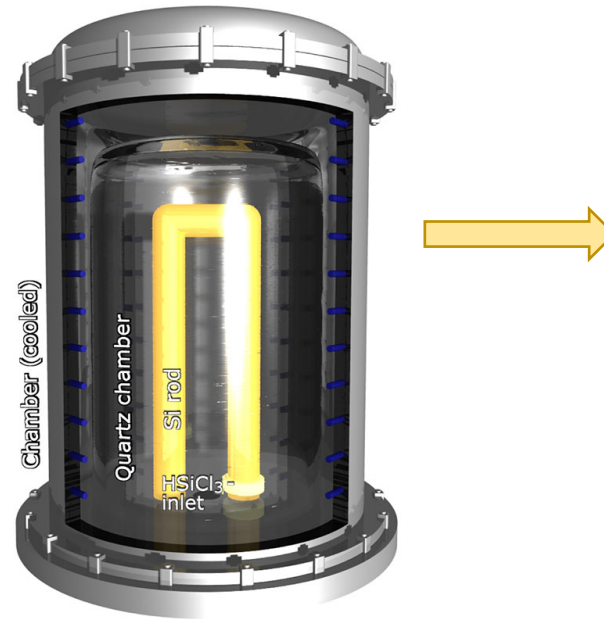
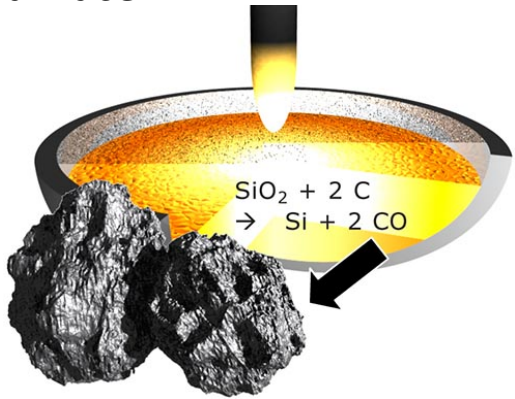
Purification of Silicon by distillation (Siemens Process)



Float-zone (Fz) Technique



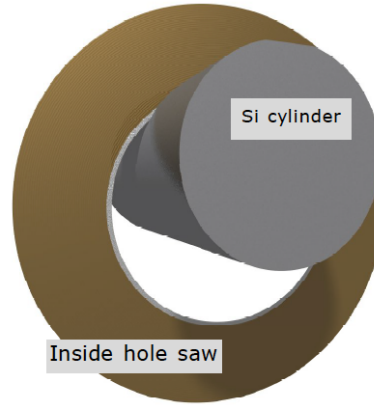
Reduction of SiO_2 with carbon to metallurgical grade silicon (>98%) in an electric arc furnace



Electronic grade poly silicon
(9N, impurities $< 10^{14} \text{ cm}^{-3}$)

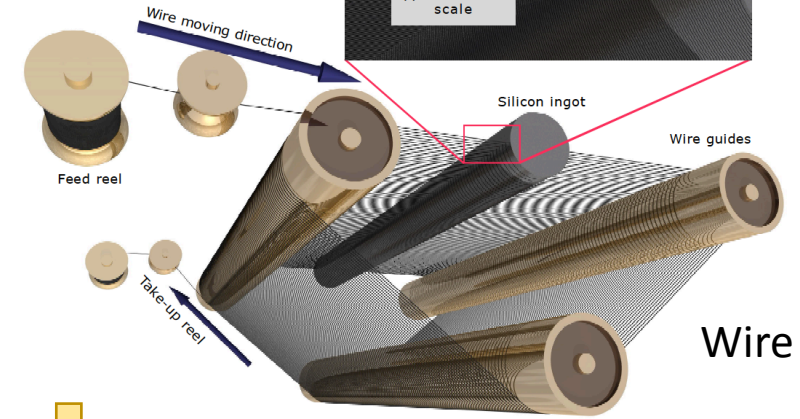
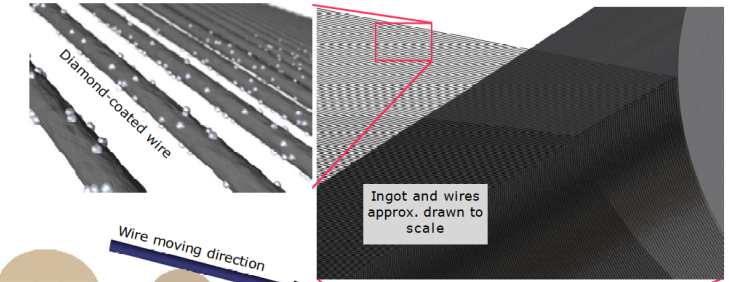
From Single Crystal to Polished Wafer

Grinding

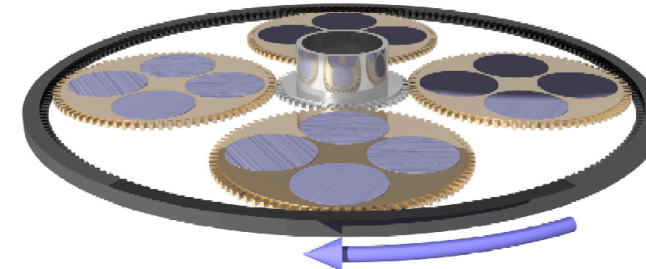
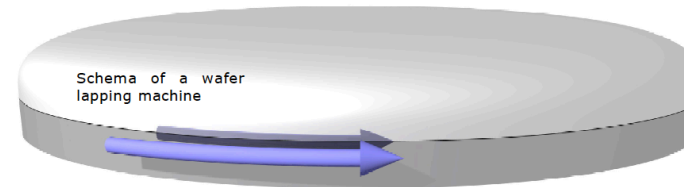


Inside Hole Saw

Dicing



Wire Saw

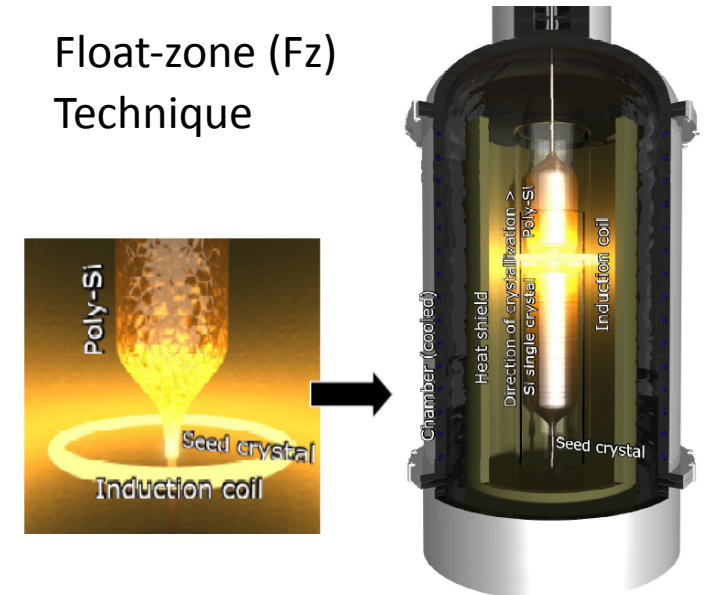
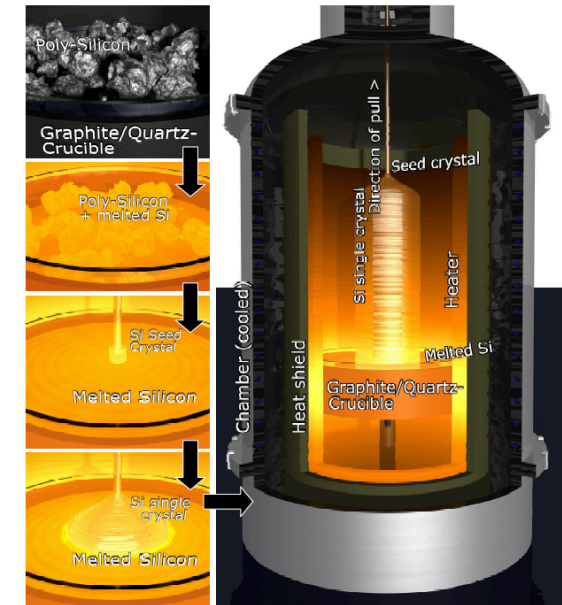
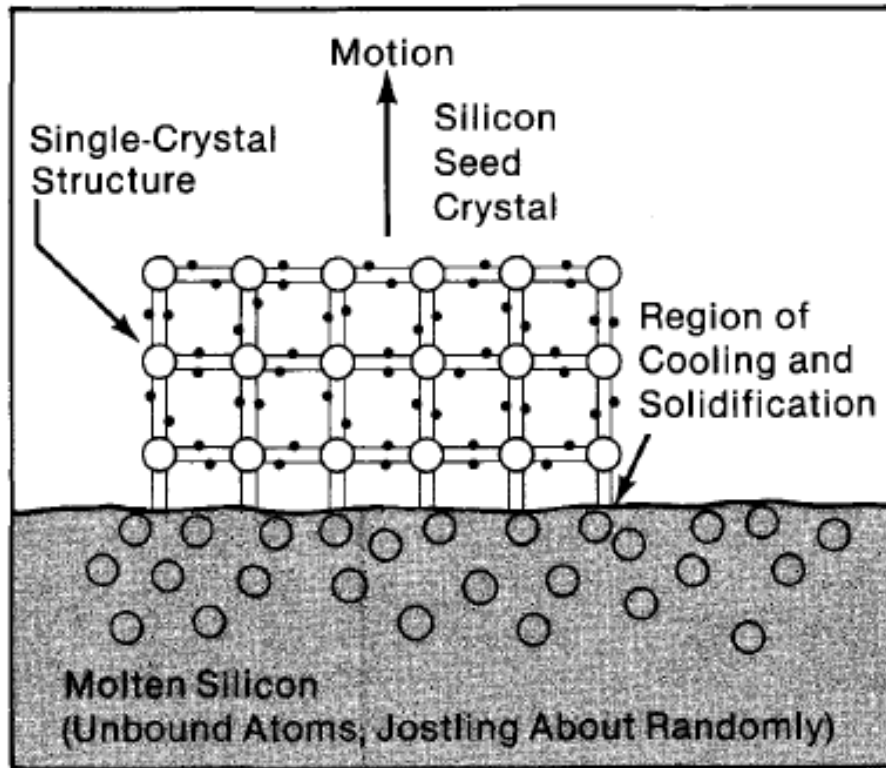


Lapping



Etching, Polishing, Cleaning

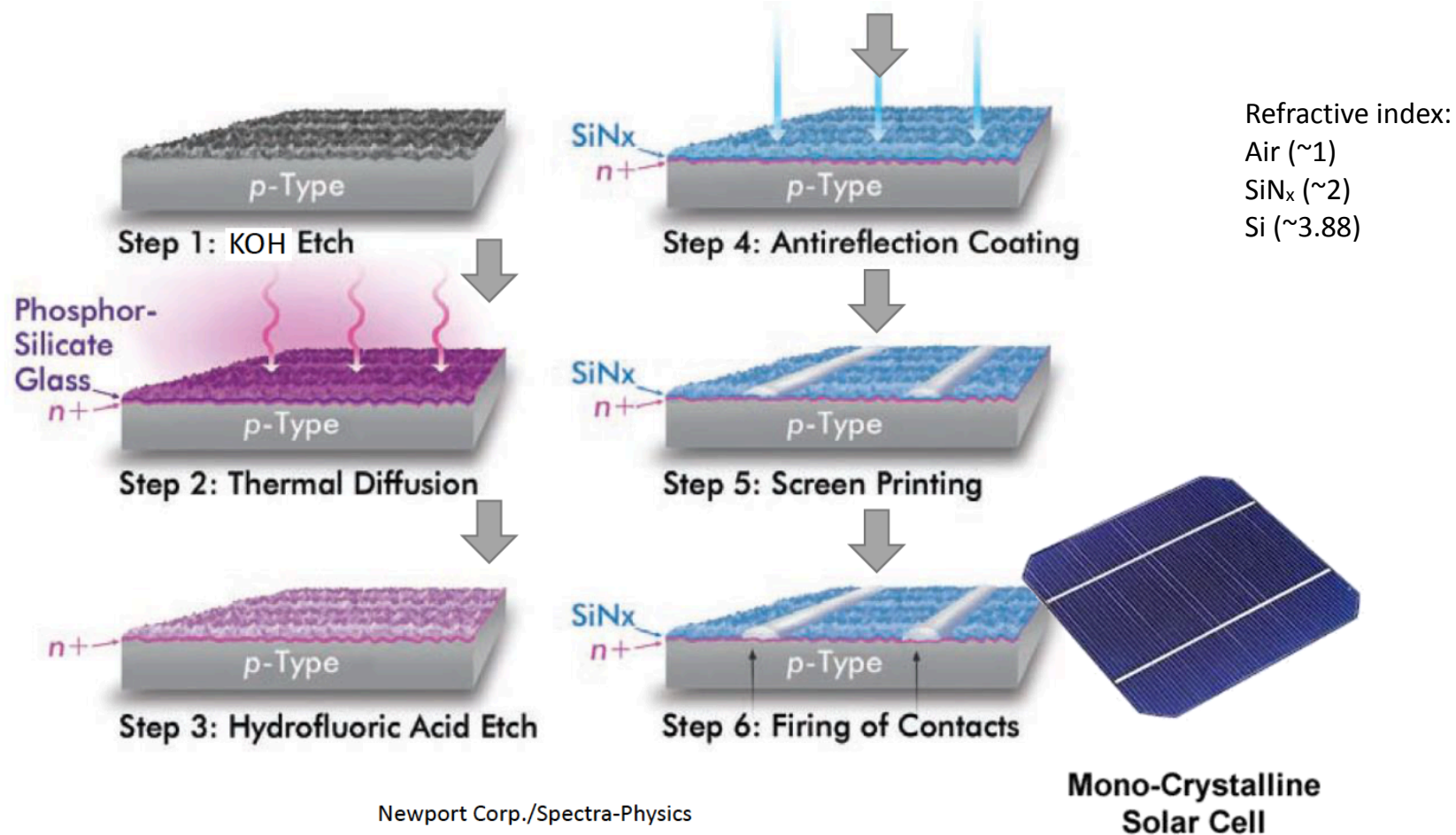




Screen Printed Solar Cells: <https://www.pveducation.org/pvcdrom/manufacturing-si-cells/screen-printed-solar-cells>

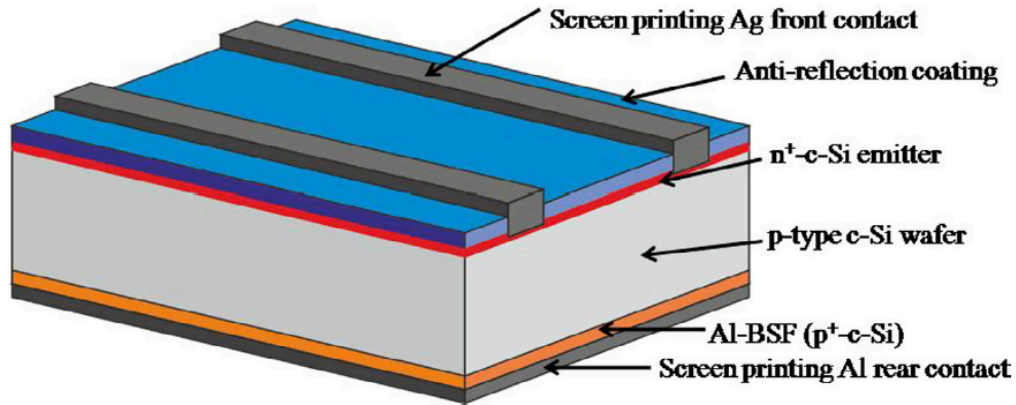
Buried Contact Solar Cells: <https://www.pveducation.org/pvcdrom/manufacturing-si-cells/buried-contact-solar-cells>

High Efficiency Solar Cells: <https://www.pveducation.org/pvcdrom/manufacturing-si-cells/high-efficiency-solar-cells>

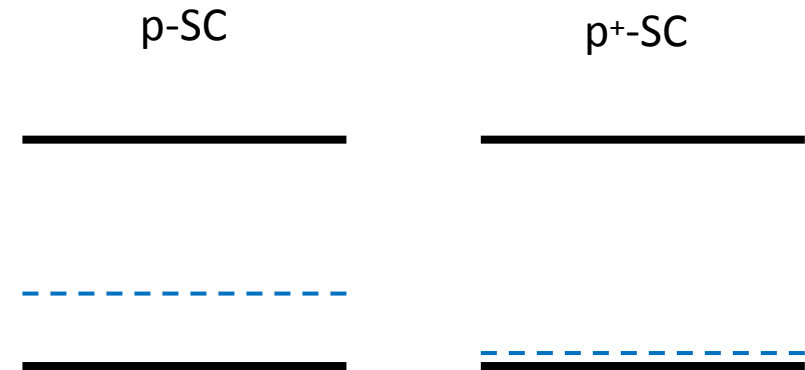
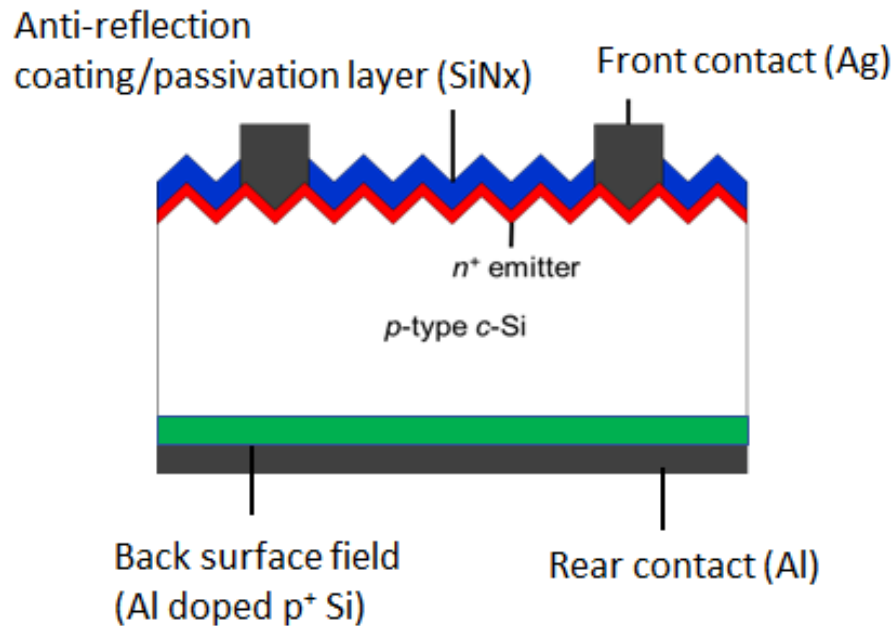


Single Crystalline Si Solar Cells Architecture

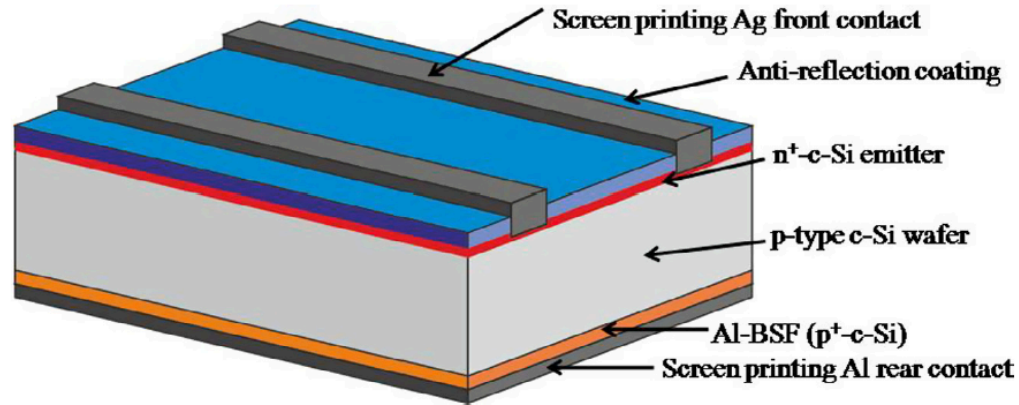
Conventional Si Solar Cell: Al-back surface field (BSF) solar cell



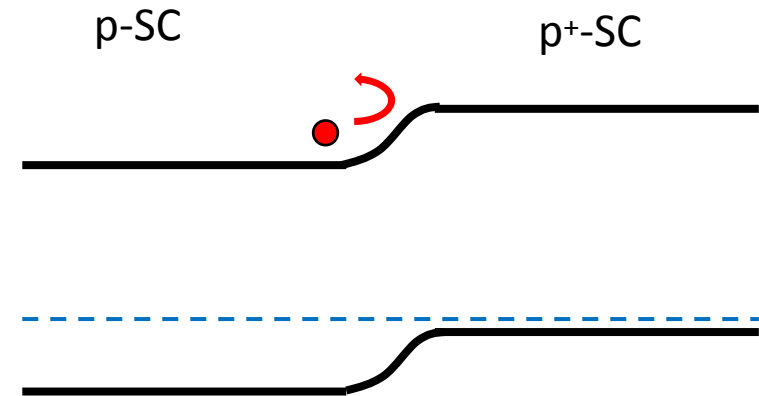
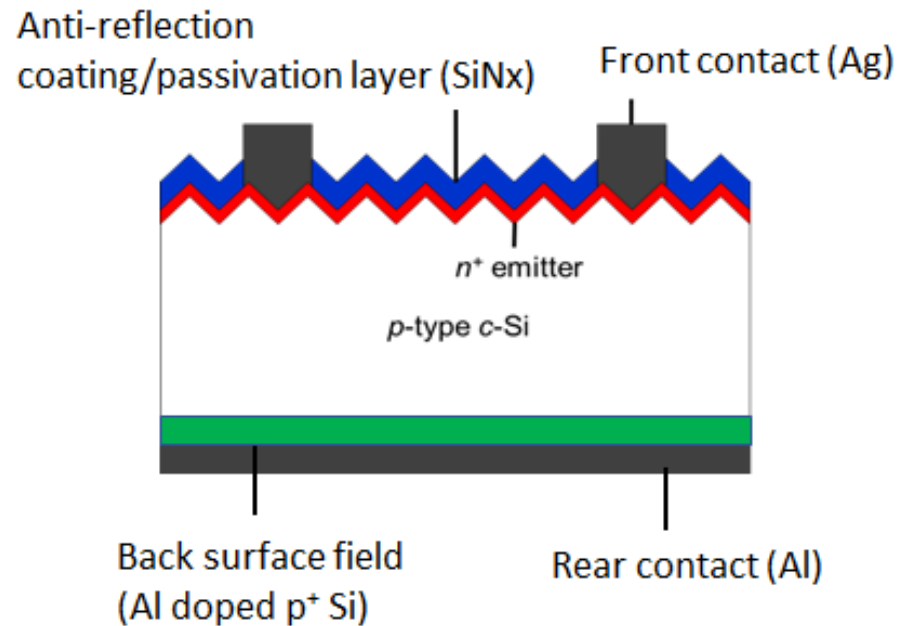
- At the rear side, a heavily Al-doped p⁺-region in p-type c-Si forms a high-low (p⁺/p) junction known as Al-BSF.
 - The potential barrier at the high-low (p⁺/p) junction drives electrons away from reaching the back electrode and towards the pn junction (Reduced surface recombination)
- Increase in V_{oc} and J_{sc} .



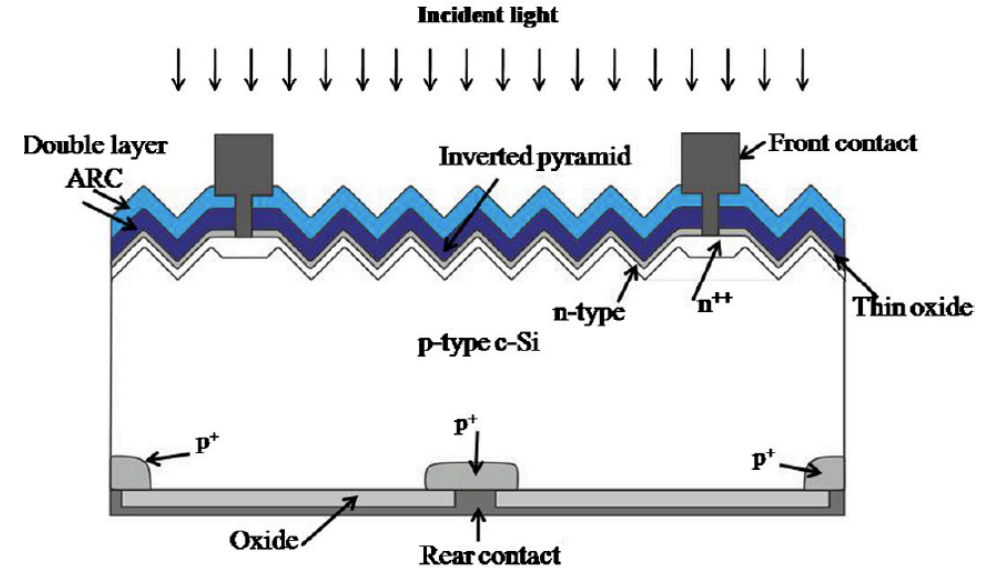
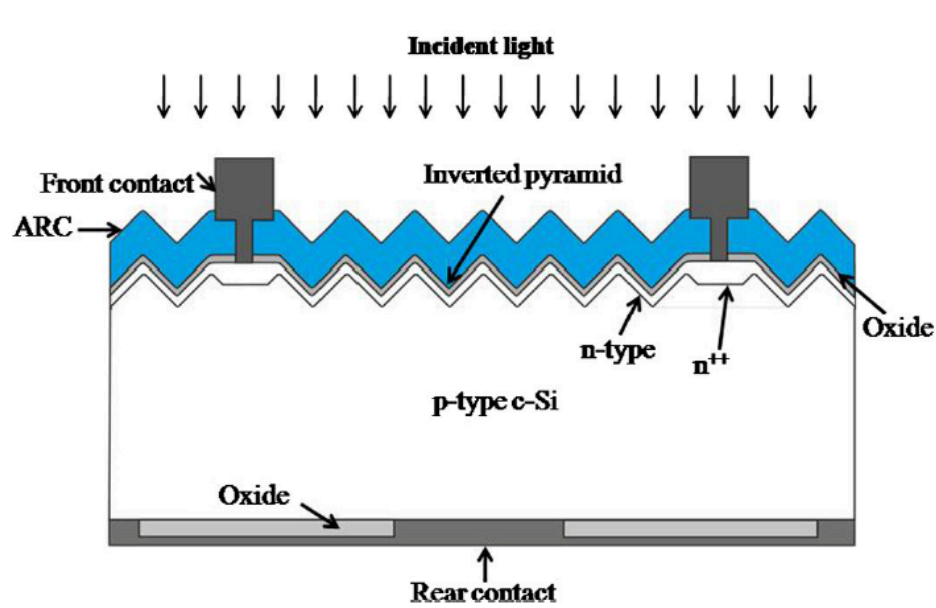
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High Efficiency Solar Cell: passivated emitter rear contact (PERC) and passivated emitter rear locally-diffused (PERL) solar cell

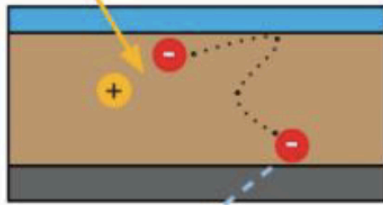


Rear side dielectric passivation layer (Al_2O_3): reduced surface recombination and improved reflection.

Electric field in the BSF region between p^+/p junction drives electrons away towards the pn junction and reduces surface recombination at the defective metal/c-Si interface.

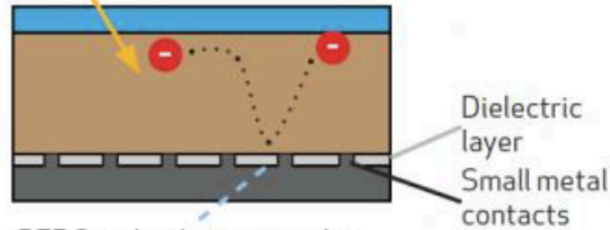
21.2% with PERC and 25% with PERL

CONVENTIONAL CELL



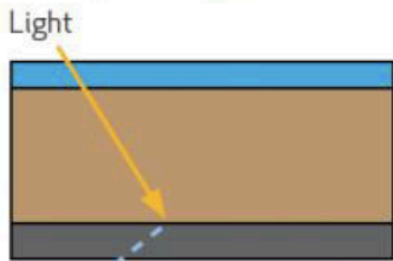
If an electron reaches the back surface, it is frequently captured and can no longer contribute to the current.

PERC CELL



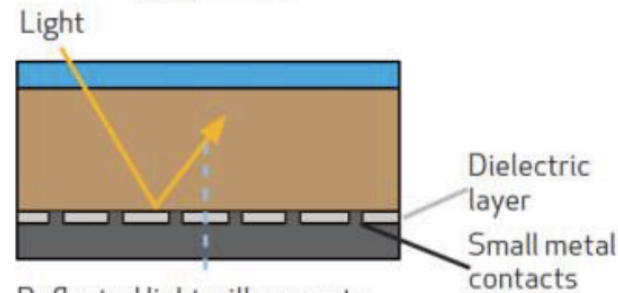
PERC technology stops the electron from being captured, and gives it a 'second chance' to reach the emitter and contribute to the current.

CONVENTIONAL CELL

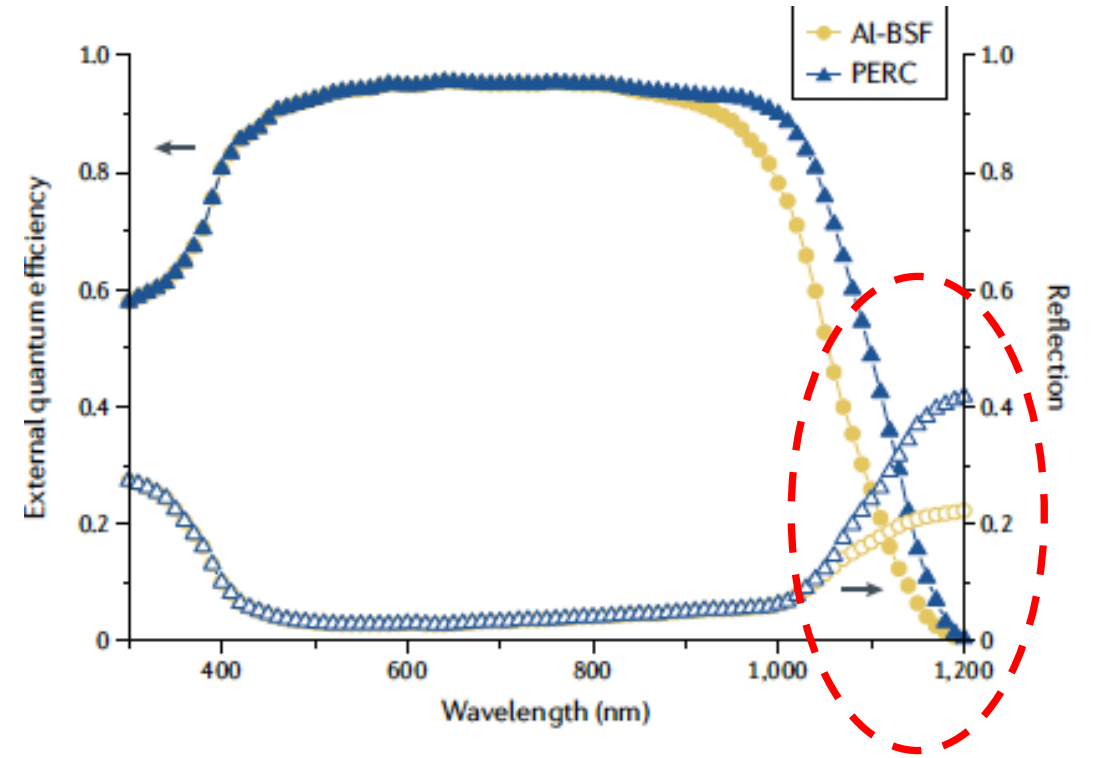


Light is absorbed by the aluminum metallization.

PERC CELL

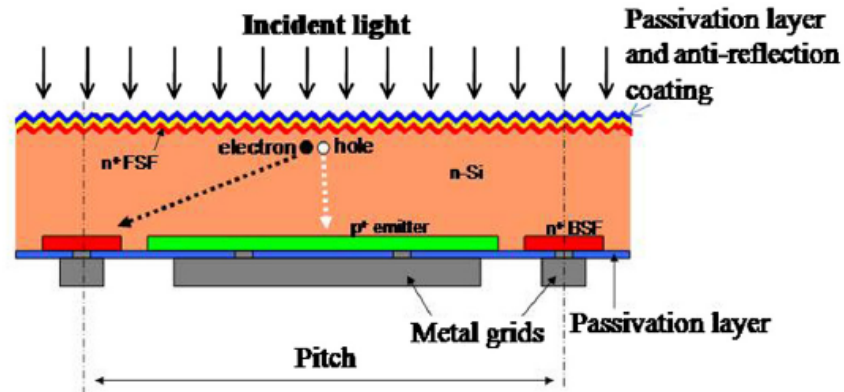


Reflected light will generate additional current.

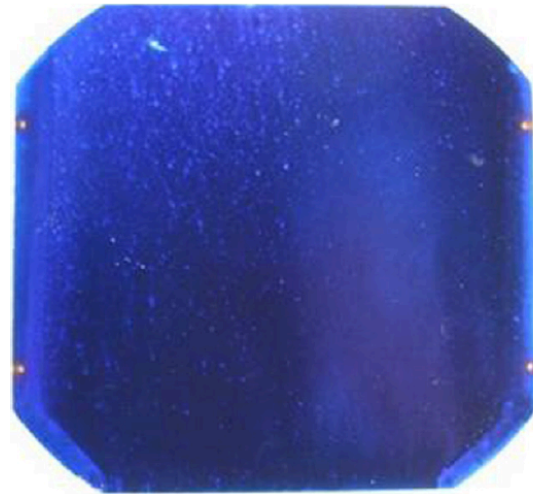
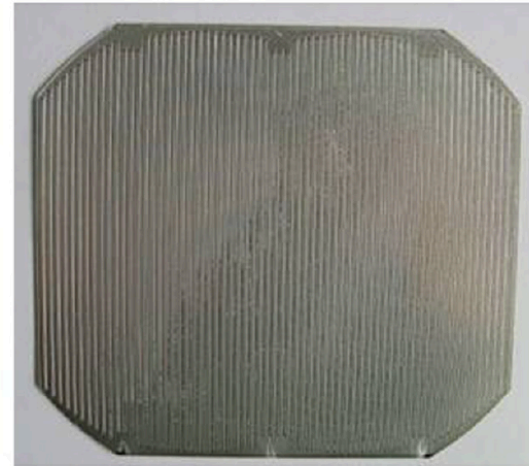


C. Ballif et al., *Nat. Rev. Mater.*, **7**, 597 - 616 (2022)

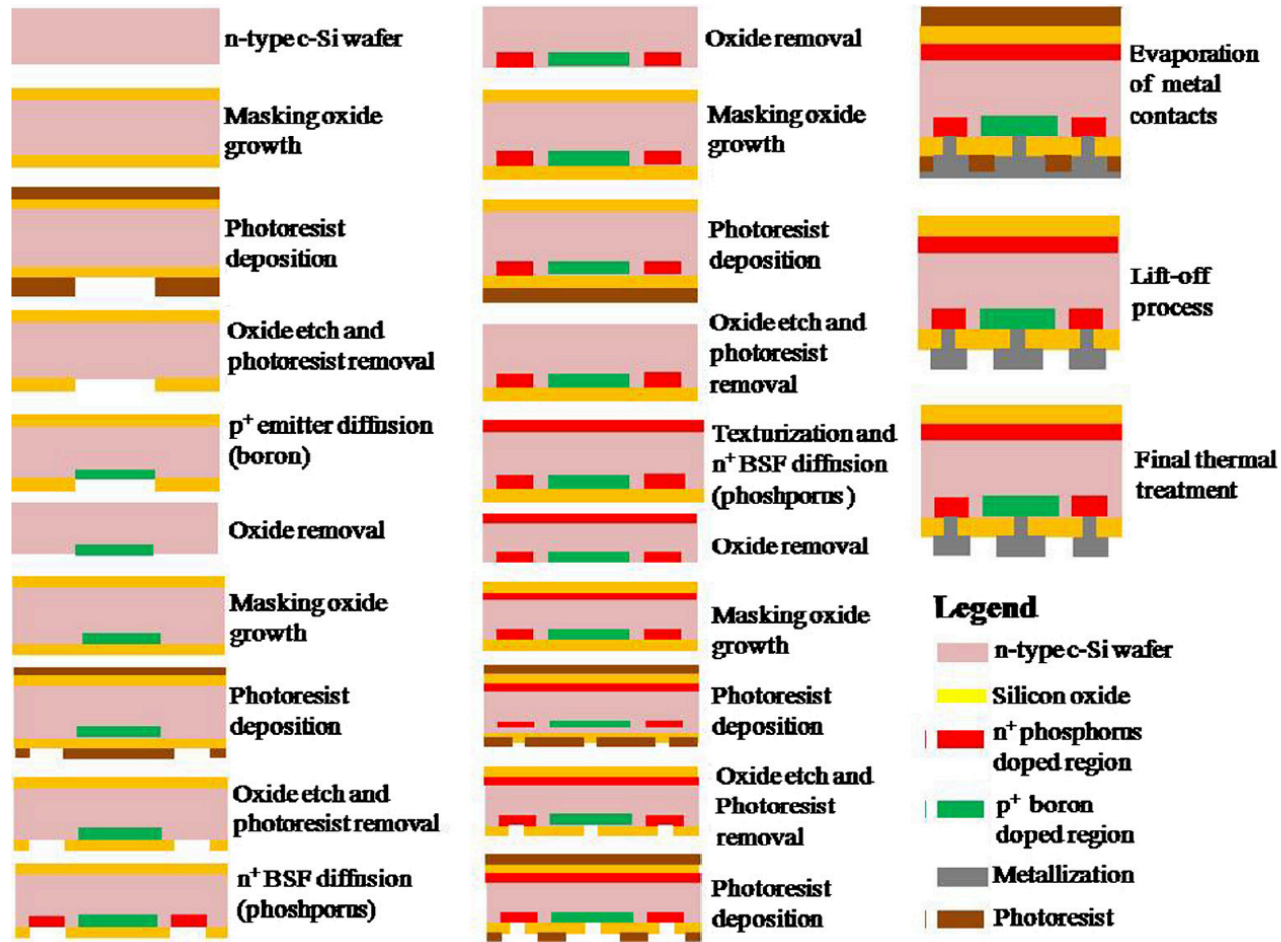
Interdigitated back contact (IBC) c-Si solar cells



- Major advantage: No front side metallization grid → Zero shading losses → High J_{sc}
- No limit for the width and thickness of metallization on the back side: Reduced series resistance
- Advantageous for the module manufacturing because of co-planar interconnection of the back-contact
- Passivation and light trapping properties can be optimized for the front side

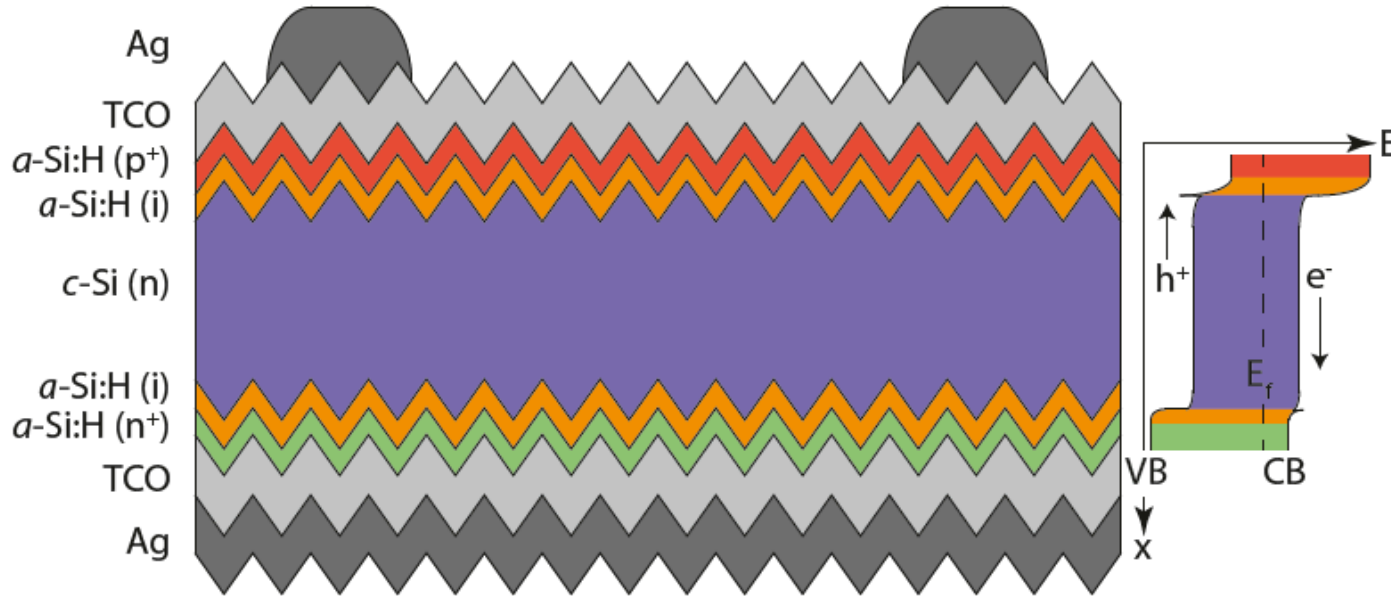
Grid less front side (147.4 cm²)

Rear side



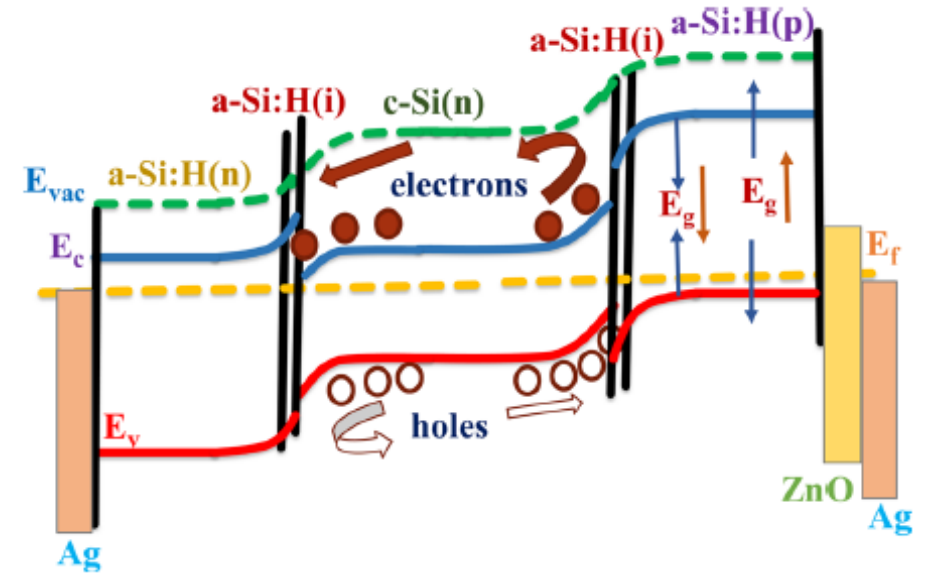
- The complexity of the processing technology: Example of a complex laboratory scale process flow for the IBC solar cell processing using photolithography and high-temperature diffusion processes.
- Photolithography is however not a cost-effective process for mass production in the photovoltaic industry.
- High accuracy masking steps are required to avoid shunting between p-type and n-type electrodes.
- Highly pure, lightly doped Fz c-Si wafers with diffusion length at the least four times higher than the thickness of the c-Si wafer and the lifetime of 1 – 3 ms are required.

Si Heterojunction solar cell



Wolf et al., *Green*, 2. 7 – 24 (2012)

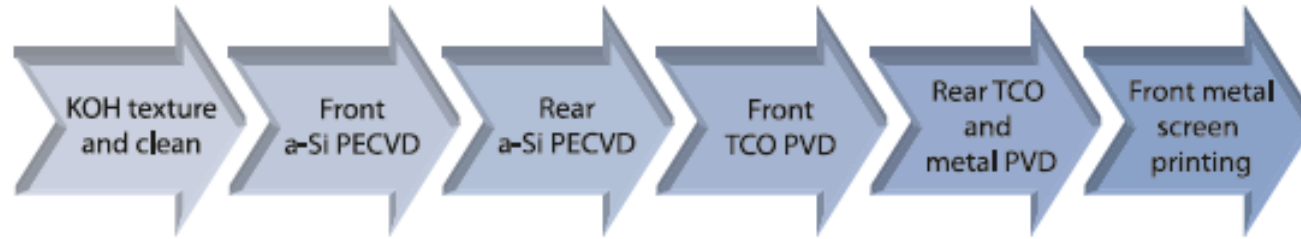
Type I Heterojunction at c-Si and a-Si:H



V. Kanneboina, *J. Comp. Electronics*, 20:344 (2021)

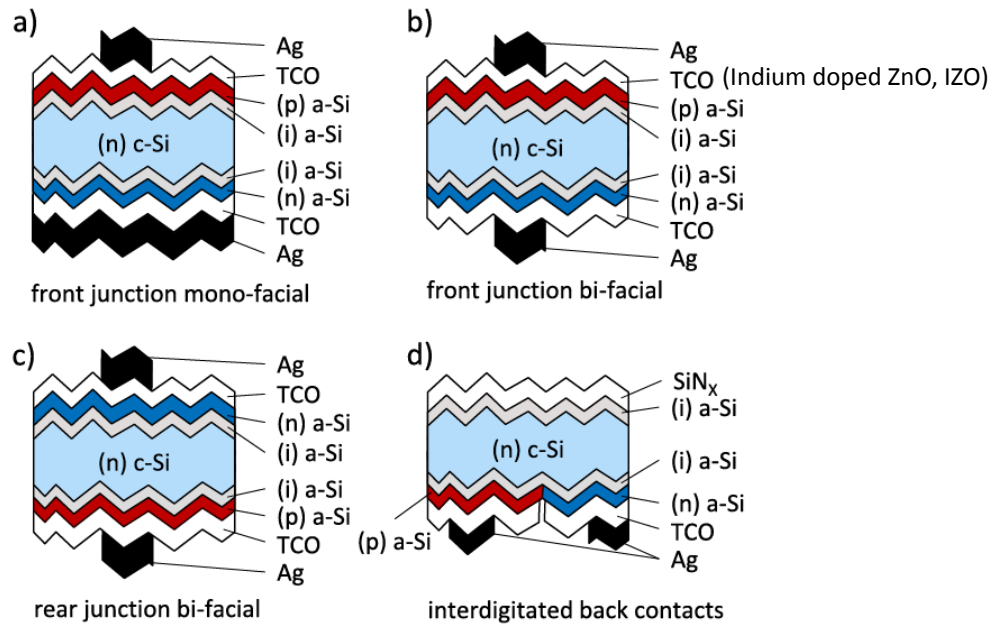
- Doped (n or p) a-Si:H over-layers are used to form junctions as electron and hole collectors, allowing the fabrication of nearly recombination-free contacts.
- Long carrier lifetime by a-Si:H over-layers
- Charges trickle through the buffer layers sufficiently slowly to build up a high voltage e.g > 730 mV.

Basic process steps for Si Heterojunction solar cell: low temperature process <200 °C

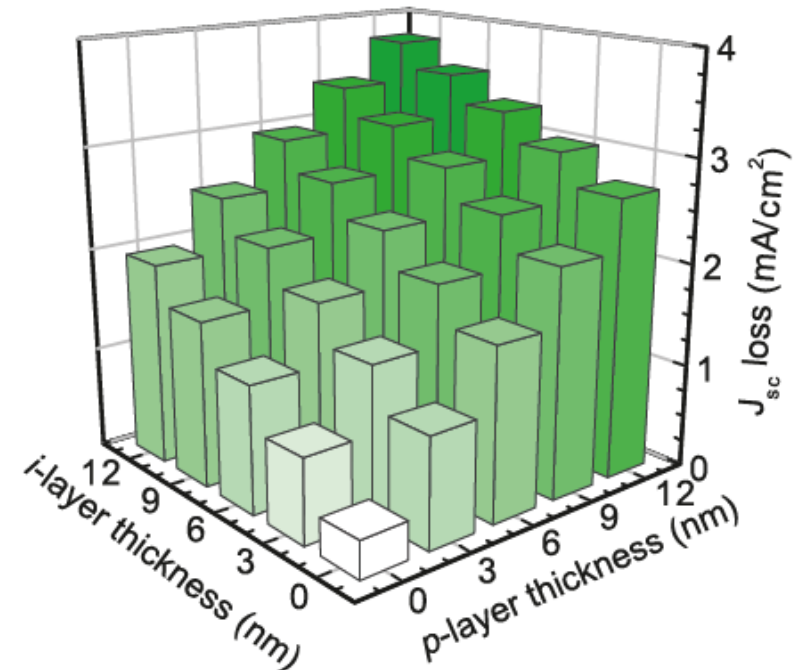


Wolf et al., *Green*, 2. 7 – 24 (2012)

Device architectures for SHJ solar cells.

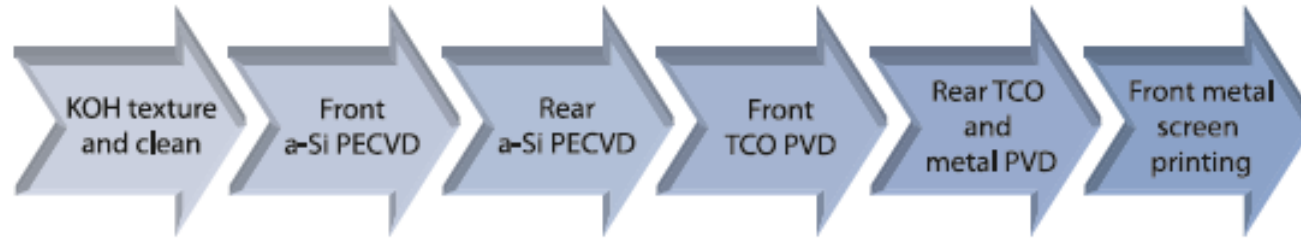


Estimate of the losses in J_{sc} below 600 nm associated with increasing intrinsic and p-type layer thicknesses: bandgap of a-Si:H (1.7–1.9 eV)



Haschke et al., *Solar Energy Mater. Solar Cells*, 187. 140 – 153 (2018)

Basic process steps for Si Heterojunction solar cell: low temperature process <200 °C

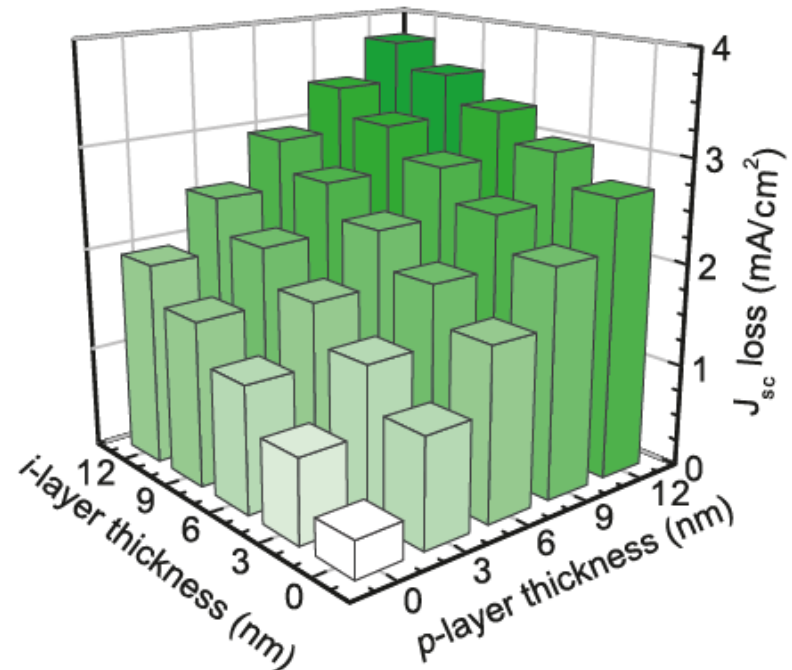


Wolf et al., *Green*, 2. 7 – 24 (2012)

Estimate of the losses in J_{sc} below 600 nm associated with increasing intrinsic and p-type layer thicknesses: bandgap of a-Si:H (1.7–1.9 eV)

Solution!

- Improving TCO transparency.
- Replacing a-Si:H with microcrystalline Si, which has features a higher doping.
- Combination with IBC structure.
- Thinner wafer (general trend for all c-Si PV technologies) possible to further increase V_{oc} .

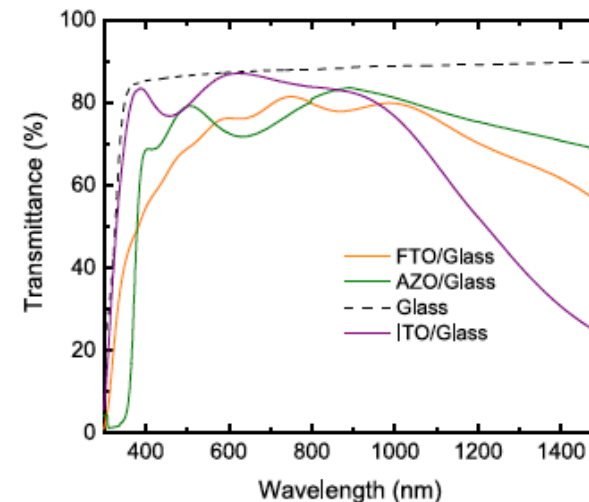


EPFL Transparent Conductive Oxides

- IZO (Indium doped Zinc Oxide)
- AZO (Aluminum doped Zinc Oxide)
- ITO (Indium doped Tin Oxide)
- FTO (Fluorine doped Tin Oxide)

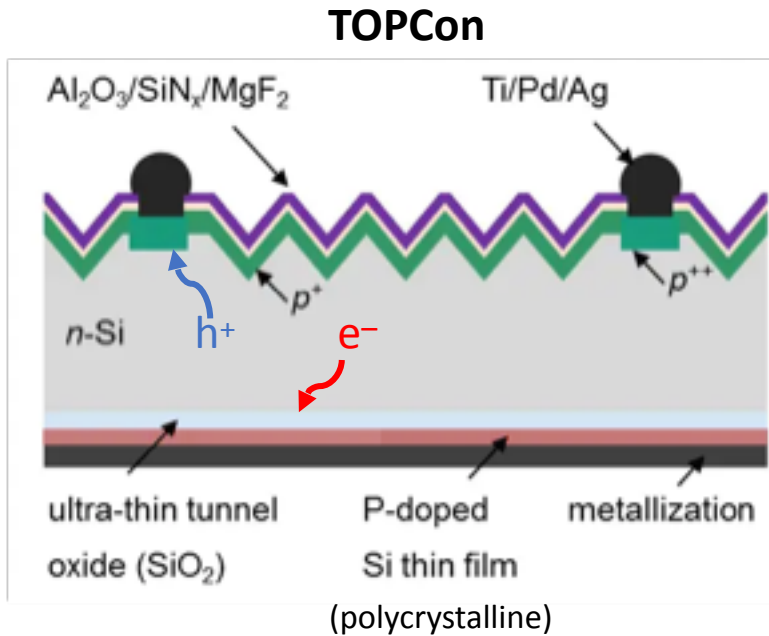


Image from <https://www.ossila.com/>



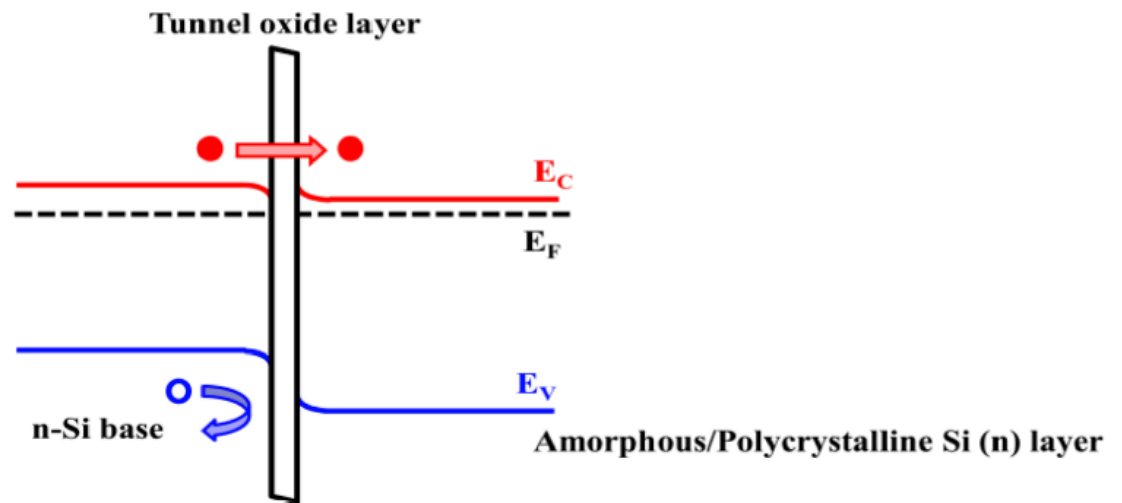
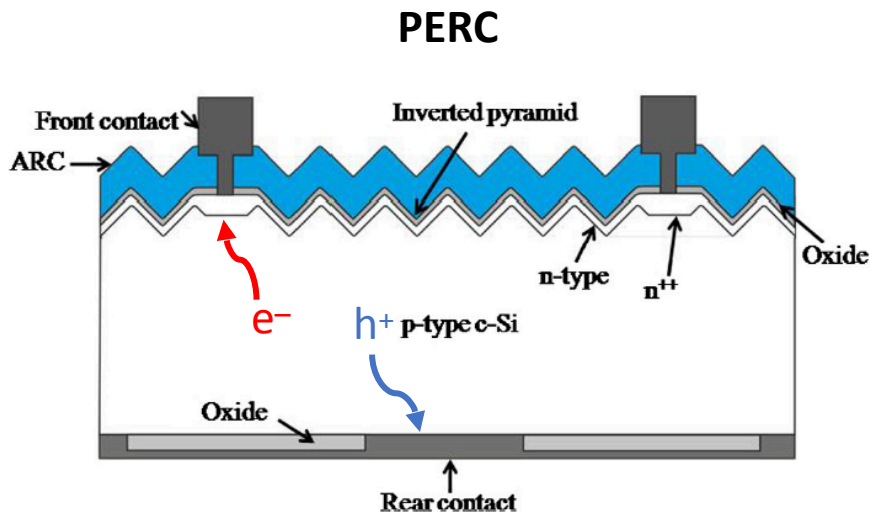
Data from V. Marinova et al., Opt. Mat.: X, 22, 100330 (2024)

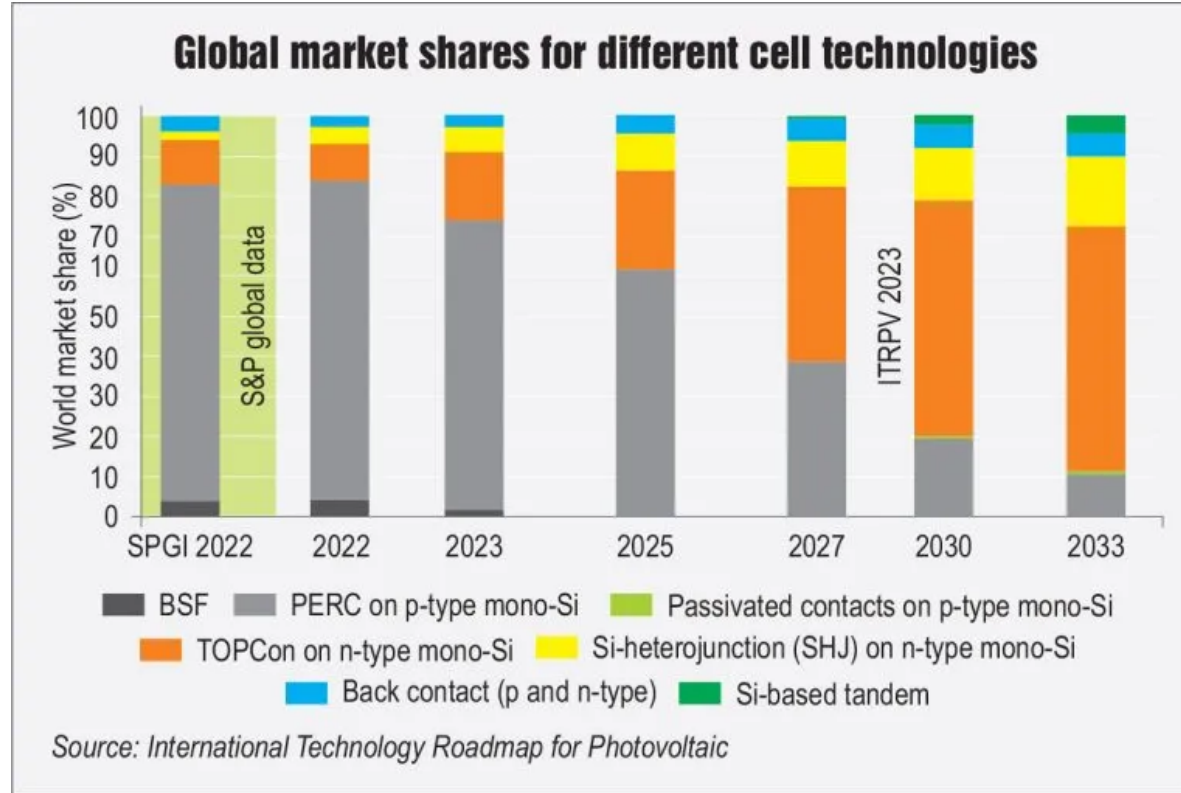
	IZO	AZO	ITO	FTO
Conductivity	Good (better than ITO)	Lower than ITO	Good	Lower than ITO
Transmittance	Good even in the NIR	Good	Good in the Vis	Good in the Vis
Thermal stability	Least	Lower than FTO	Lower than AZO	Good
Structure	Amorphous	Polycrystalline	Polycrystalline	Polycrystalline
Deposition method	Sputtering, Atomic Layer Deposition, CVD	Sputtering, Atomic Layer Deposition, CVD	Sputtering, Electron beam evaporation	Spray pyrolysis, Chemical vapor deposition (CVD)
Cost	High	Low	High	Low



- The term TOPCon stands for **Tunnel Oxide Passivated Contact** and the architecture was presented by researchers at the Fraunhofer Institute for Solar Energy Systems in Freiburg in 2013.
- The heavily phosphorous doped poly-Si(n) layer induces a band bending in c-Si(n) absorber .
- The thin oxide could have a slightly asymmetric tunnelling probability for electrons and holes due to differences in energy barrier heights.

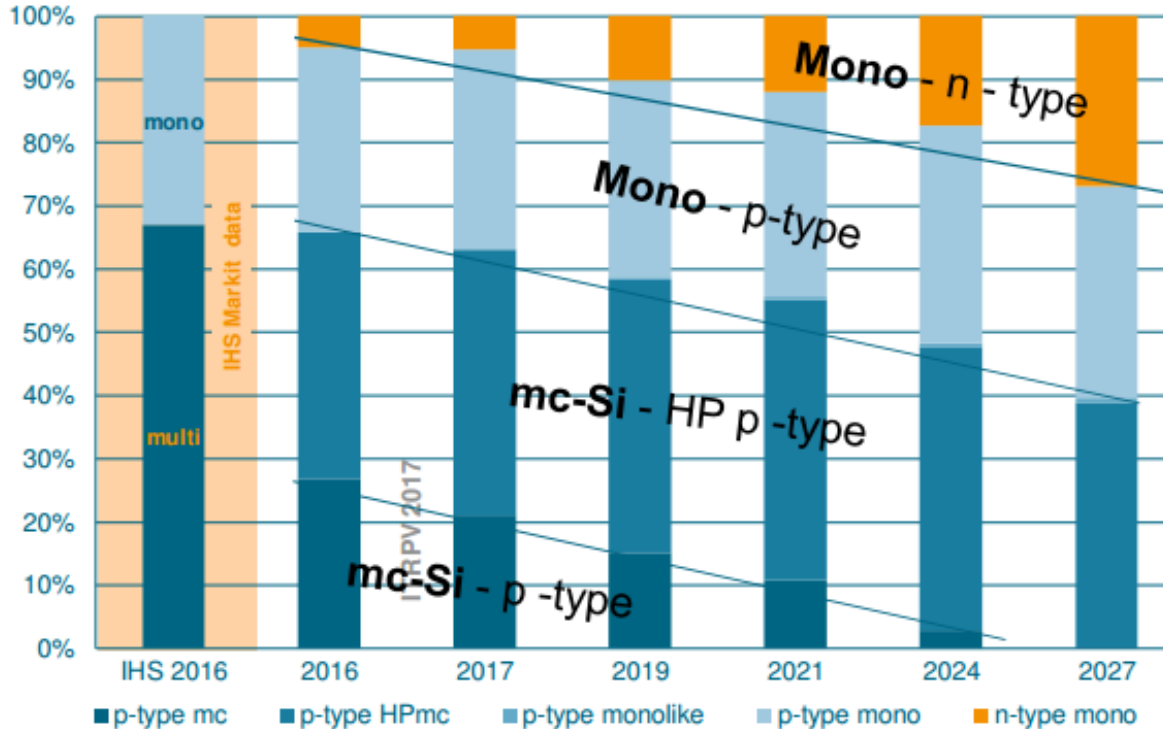
$$(\Delta\Phi_e < \Delta\Phi_h)$$



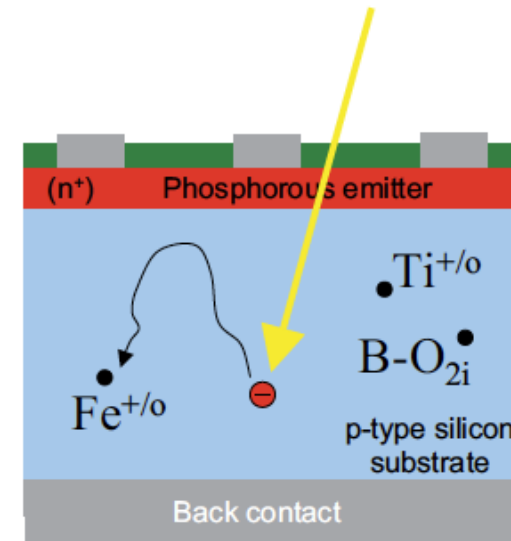


	PERC	TOPCon	SHJ	IBC
Efficiency in mass production	23.50 %	24.80 %	25.80 %	25.00 %
Efficiency limit	24.50%	28.70%	28.70%	29.10%
Complexity on fabrication	★★	★★★★	★	★★★★★
Facility investment	★	★★	★★★★	★★★★★

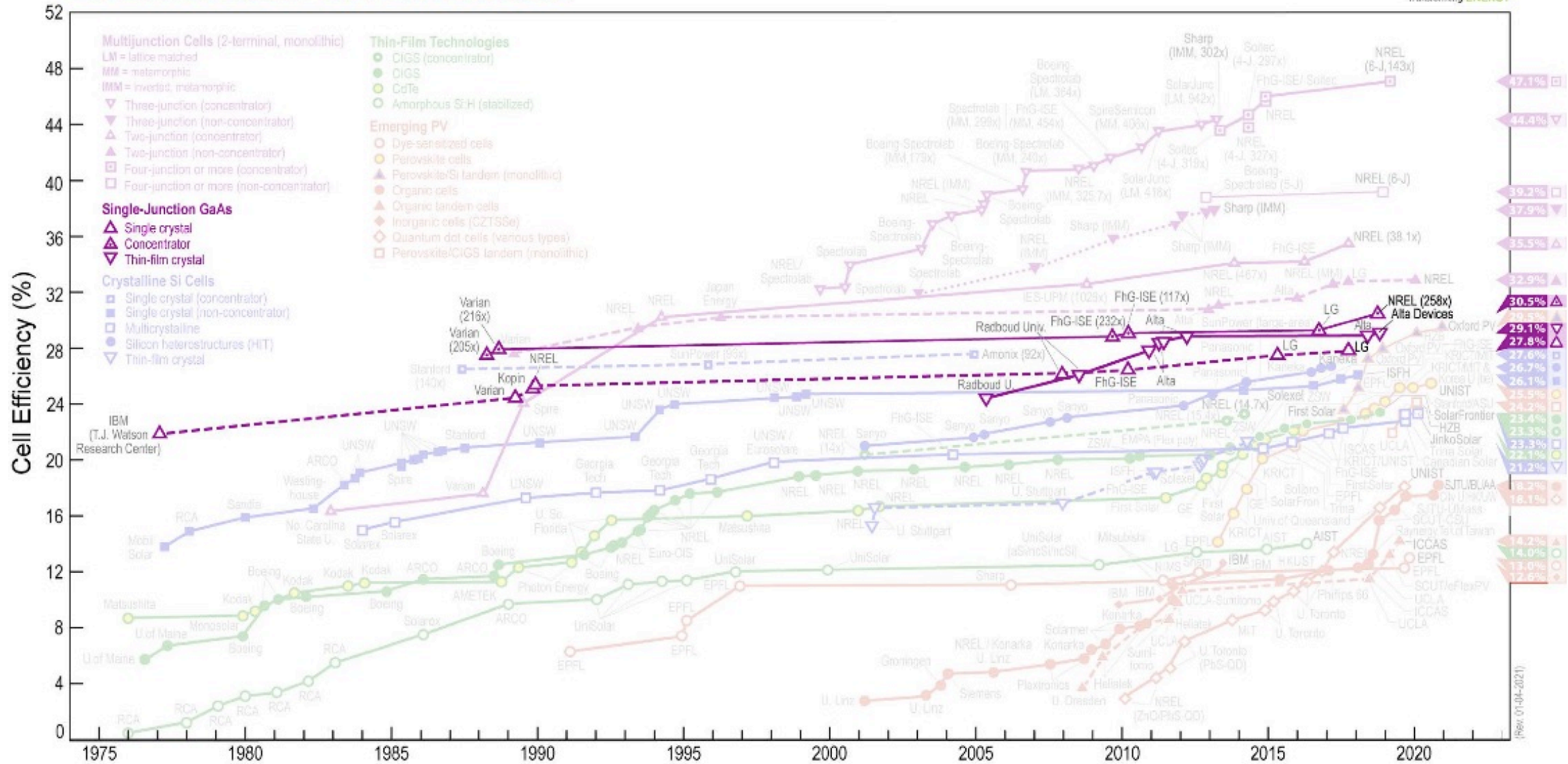
Trend: share of c-Si material types



- Boron doped p-type Cz wafer: Boron (dopant) and oxygen (growth process impurity) forms a boron-oxygen related metastable defect upon illumination.
 → Solution: Boron to Gallium dopant
 FZ instead of Cz
 Regeneration process to remove the defect
- Transition metal defects, Fe in p-type wafers have an increased capture rate for minority carriers in p-type wafers (e⁻).

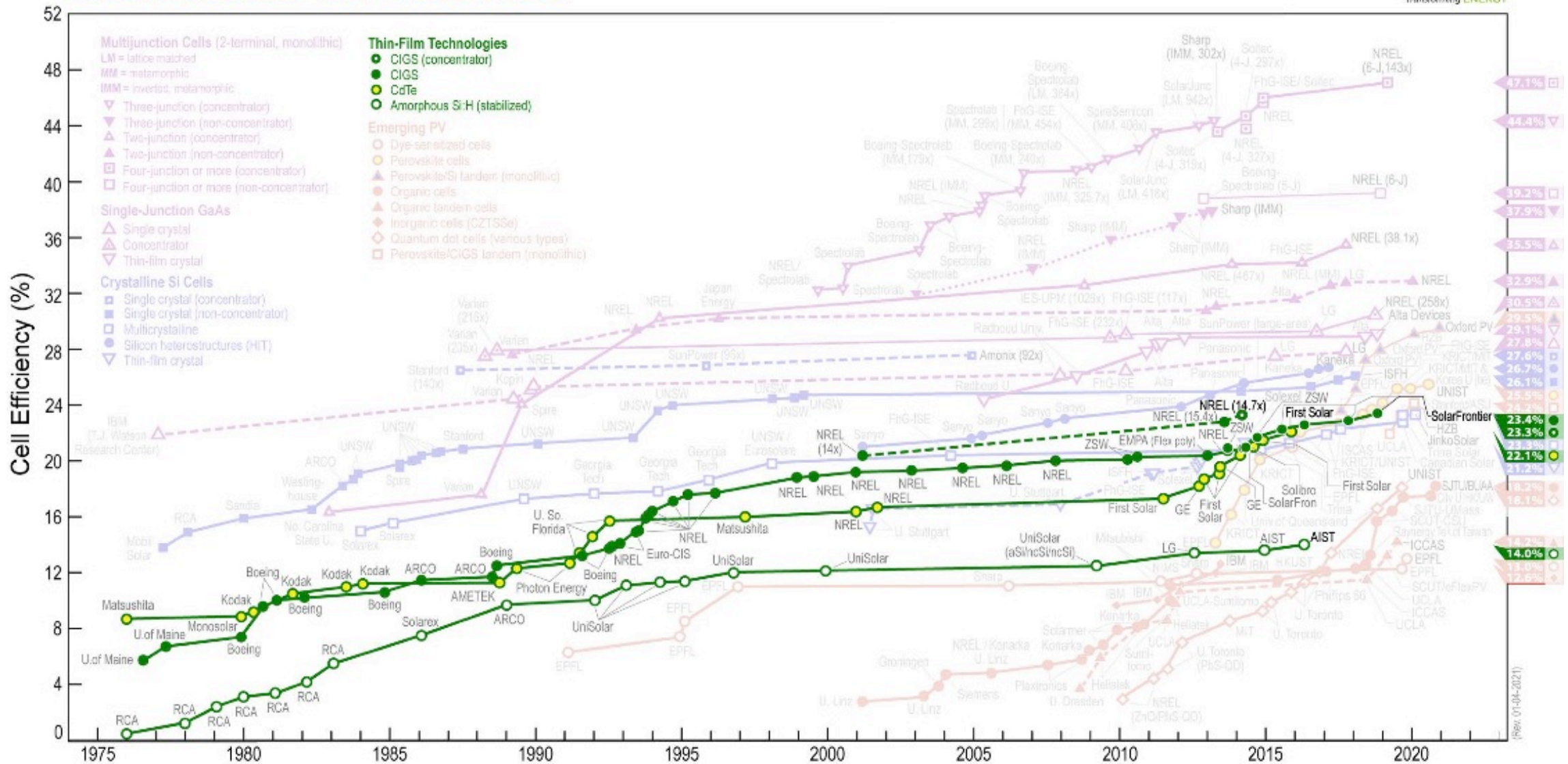


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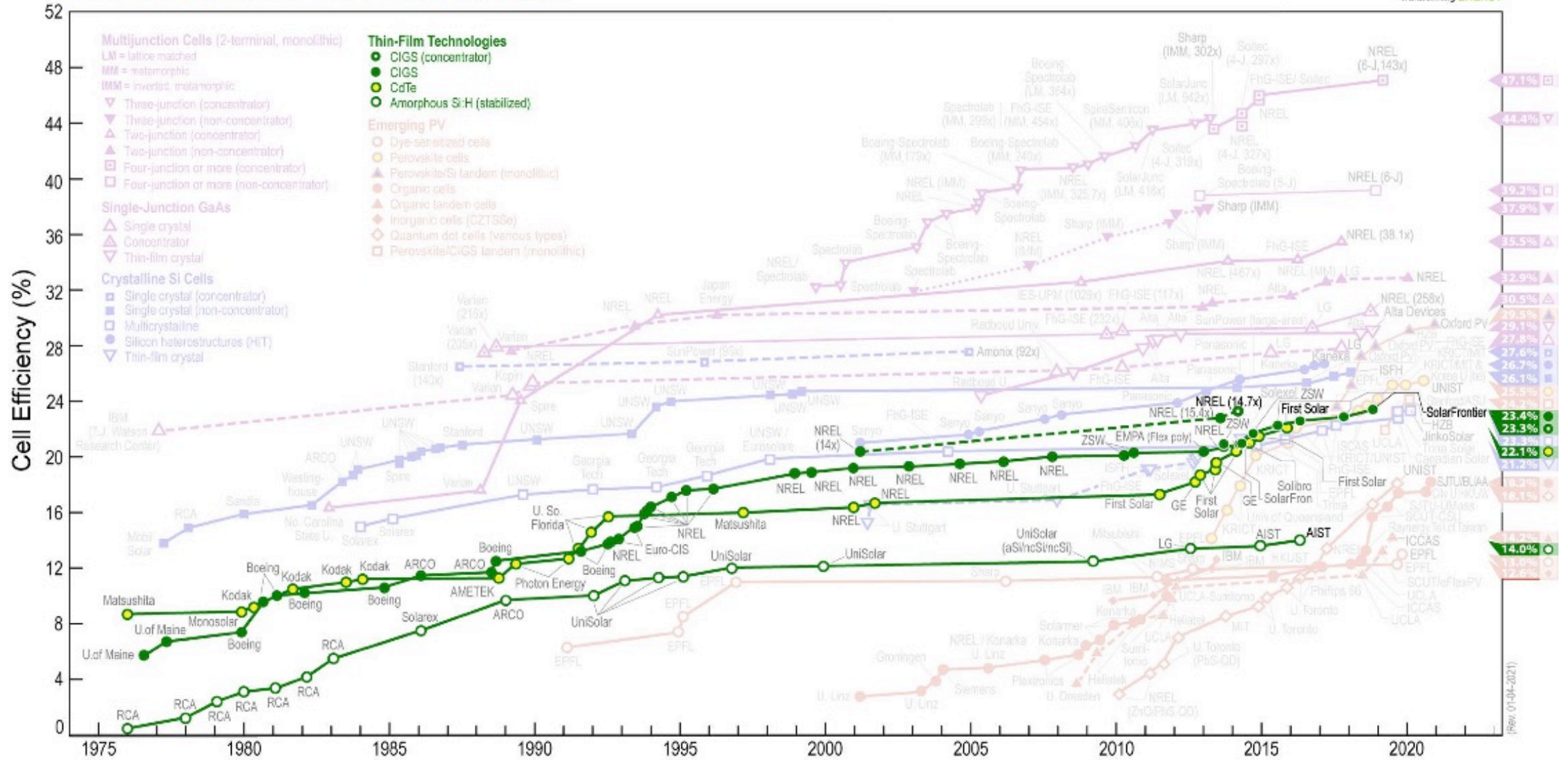


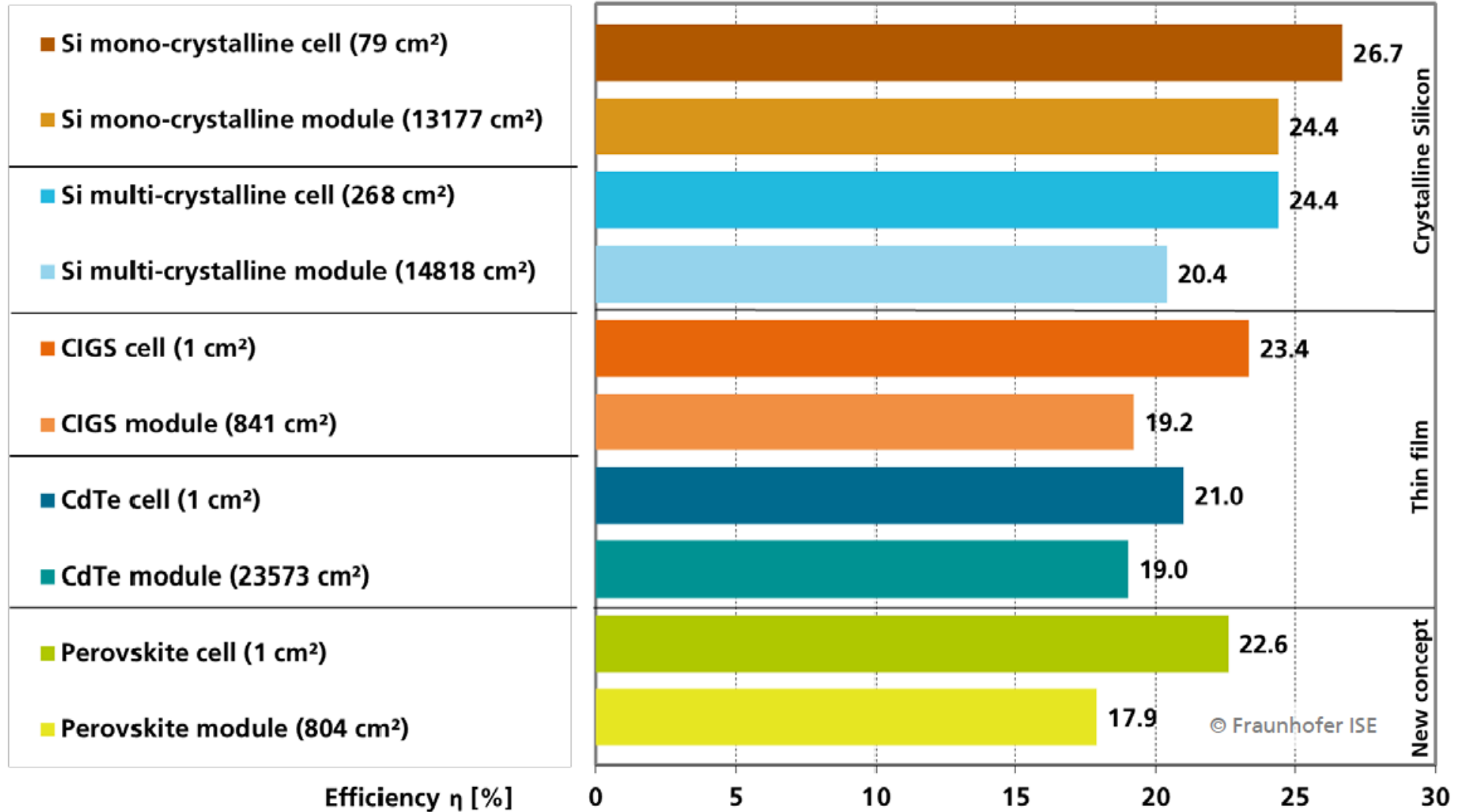
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Slides from Fraunhofer Institute, ISE, prepared by Dr. Simon Philipps and Werner Warmuth